

MemoryTen

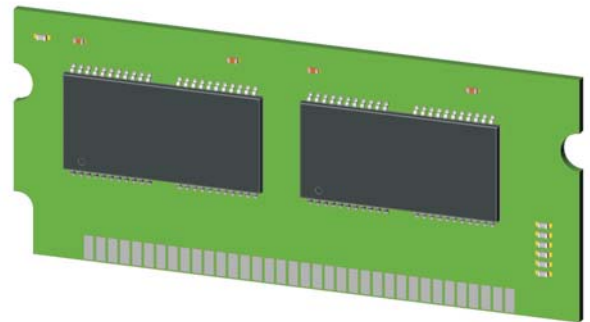
8L4E116-60-OKI 2 Meg X 32 EDO 72 Pin SODIMM 60ns 1K Refresh 3.3V

Features

- JEDEC standard 72 pin Small Outline Dual Inline Memory Module (SODIMM),
- JEDEC standard PDPin & Pinout
- 8MB (2 Meg x 32), single bank
- Single 3.3V power supply
- Extended Data Output (EDO) Mode operation
- CAS* - before - RAS* (CBR) & hidden refresh capable
- RAS* Only refresh capable
- 1664 ms, 1024-cycle refresh interval
- TTL-compatible inputs and outputs
- PCB: Height (1000mil)
- PCB: Gold-lead fingers standard

72-Pin SODIMM (MO-160b)

1.0" tall



Representative assembly

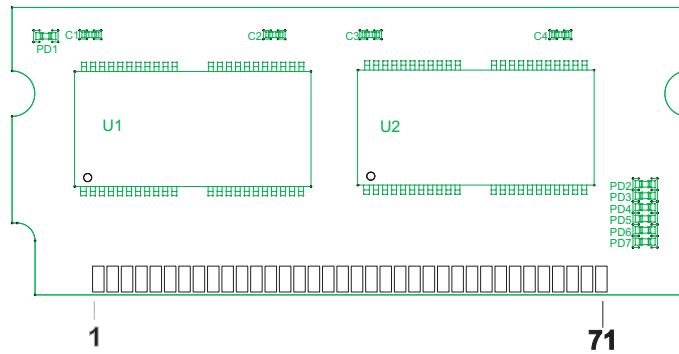
ORDERING INFORMATION

Part Number	Density	Speed	Mode	Refresh	Module Config	Chip Density	Voltage
8L4E116-60-OKI	8MB	60 ns	EDO	1K	2Mx32	1Mx16	3.3

PRODUCTION DATA information is current as of publication date.
 Products conform to specifications per the terms of MemoryTen
 standard warranty. Production processing does not necessarily include
 testing of all parameters.

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 REVA
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ALL SPECIFICATIONS FOR PRODUCTS DISCUSSED HEREIN ARE SUBJECT TO CHANGE BY MemoryTen WITHOUT NOTICE.



Pin Assignment, (72 pin SODIMM)

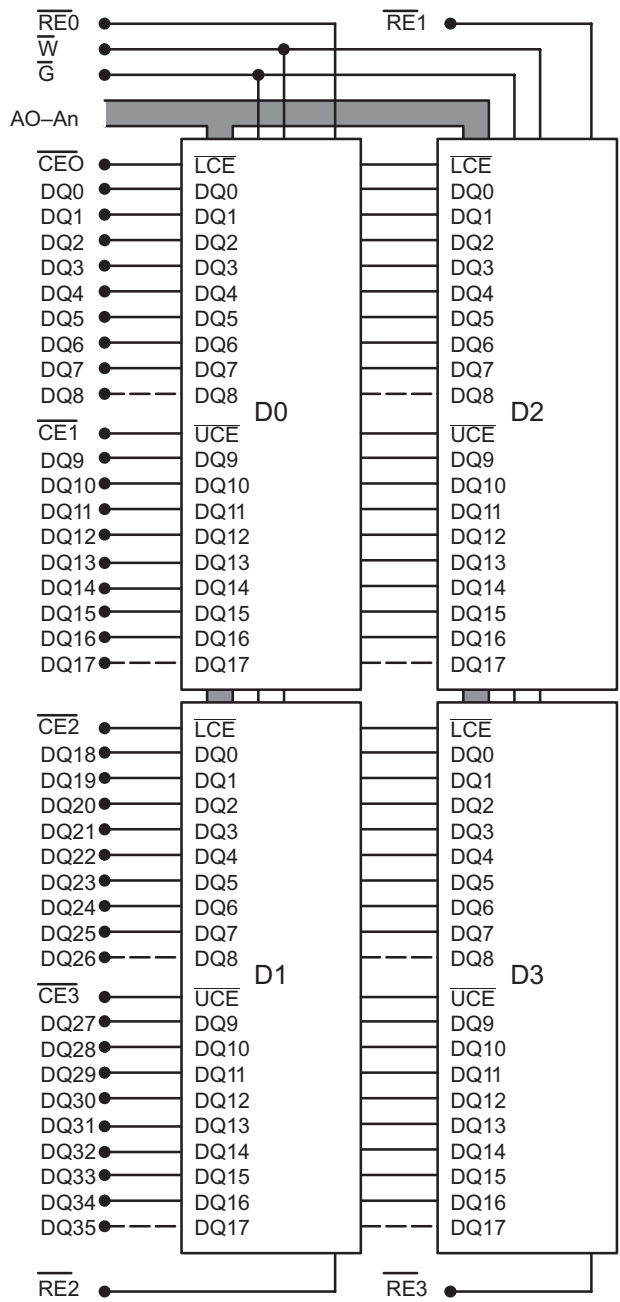
Pin	Symbol	Pin	Symbol
1	V _{ss}	37	DQ18
2	DQ0	38	DQ19
3	DQ1	39	V _{ss}
4	DQ2	40	CAS0*
5	DQ3	41	CAS2*
6	DQ4	42	CAS3*
7	DQ5	43	CAS1*
8	DQ6	44	RAS0*
9	DQ7	45	RAS1*
10	V _{cc}	46	A12
11	PD1	47	W*
12	A0	48	A13
13	A1	49	DQ20
14	A2	50	DQ21
15	A3	51	DQ22
16	A4	52	DQ23
17	A5	53	DQ24
18	A6	54	DQ25
19	A10	55	NC
20	NC	56	DQ27
21	DQ9	57	DQ28
22	DQ10	58	DQ29
23	DQ11	59	DQ31
24	DQ12	60	DQ30
25	DQ13	61	V _{cc}
26	DQ14	62	DQ32
27	DQ15	63	DQ33
28	A7	64	DQ34
29	A11	65	NC
30	V _{cc}	66	PD2
31	A8	67	PD3
32	A9	68	PD4
33	RAS3*	69	PD5
34	RAS2*	70	PD6
35	DQ16	71	PD7
36	NC	72	V _{ss}

Pin Names

Pin Name	Function
A0 – A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
W*	Read/Write Enable* (active low)
RAS0*-RAS3*	Row Address strobes (active low)
CAS0*-CAS3*	Column Address Strobes (active low)
PD1-PD7	Presence Detect
V _{cc}	Power (+3.3/5V)
V _{ss}	Ground
NC	No Connect

Presence Detect Pins Options 8MB

Pin	60 nS
PD1	NC
PD2	VSS
PD3	NC
PD4	VSS
PD5	NC
PD6	NC
PD7	NC



X32 DRAM SOSIMM, 2 Banks with X16 DRAMs

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to +4.6	V
Voltage on VCCsupply relative to Vss	V _{CC}	-1 to +4.6	V
Storage Temperature	T _{stg}	-55 to +125	°C
Operating Temperature	T _a	0 to 70	°C
Power Dissipation	P _d	2	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_a = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL}	-0.3	-	0.8	V

The following DC and AC parameters are typical. Differences may exist from one memory device vendor to another as well as small differences from one die revision to another.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Mode	Speed	8MB		Units
			Min	Max	
I _{CC1}	3.3V	60 ns	-	302	mA
I _{CC2}		Don't care		4	mA
I _{CC3}	3.3V	60 ns	-	302	mA
I _{CC4}	3.3V	60 ns	-	220	mA
I _{CC5}		Don't care		600	
I _{CC6}	EDO	60 ns	-	302	mA
I _{I(L)}		Don't care	-20	20	uA
I _{O(L)}			-5	5	uA
V _{OH}		Don't care	2.4	-	V
V _{OL}			-	.4	V

I_{CC1}: Operating Current* (RAS*, CAS*, Address cycling @t_{RC}=min)

I_{CC2}: Standby Current (RAS*=CAS*=W*=V_{in})

I_{CC3}: RAS* Only Refresh Current* (CAS*=V_{IH}, RAS* cycling @t_{RC}=min)

I_{CC4}: Hyper Page Mode Current* (RAS*=V_{IL}, CAS* cycling: t_{HPC}=min)

I_{CC5}: Standby Current (RAS*=CAS*=W*=V_{CC}-0.2V)

I_{CC6}: CAS*-before-RAS* Refresh Current* (RAS* and CAS* cycling @ t_{RC}=min)

I_{I(L)}: Input leakage current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other input pins not under test =\ 0V)

I_{O(L)}: Output leakage Current (DataOut is disabled. 0V≤V_{out}≤V_{CC})

V_{OH}: Output high Voltage Level (I_{OH} = -5mA)

V_{OL}: Output Low Voltage Level (I_{OL} = 4.2 mA)

AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$)

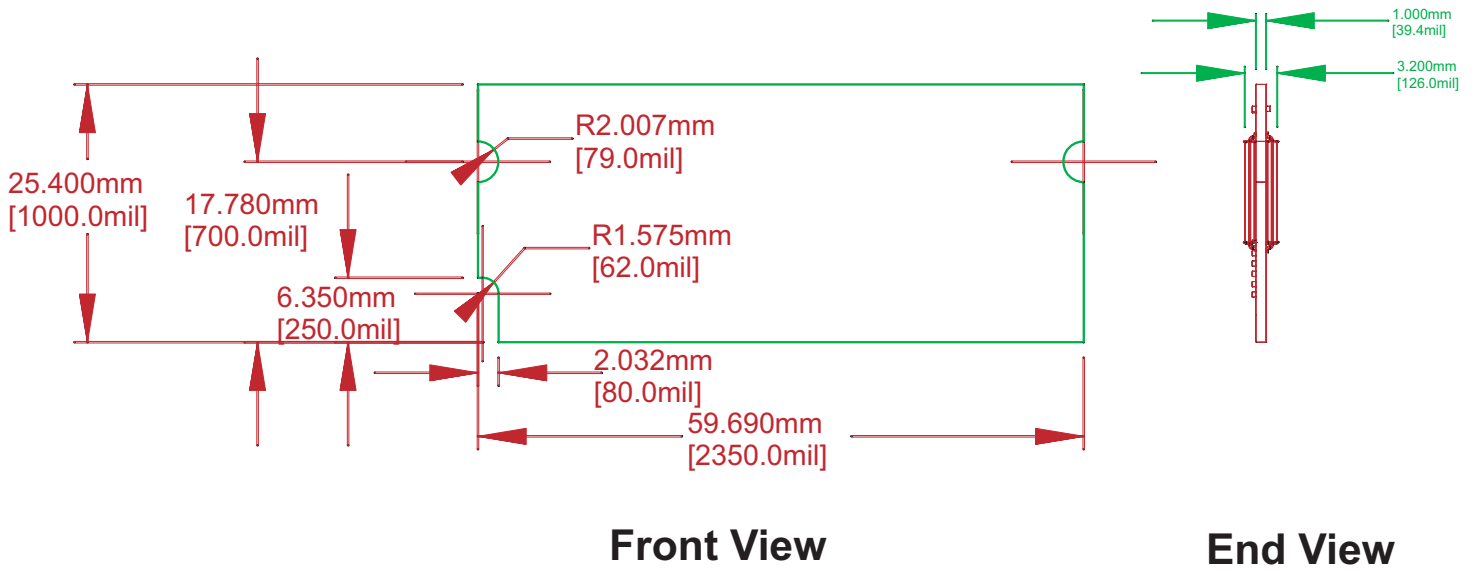
Parameter	Symbol	60 nS		Unit	Note
		Min	Max		
Random read or write cycle time	t _{RC}	110		ns	
Access time from RAS	t _{RAC}	60		ns	3,4,10
Access time from CAS	t _{CAC}	15		ns	3,4,5
Access time from column address	t _{AA}	30		ns	3,10
CAS to output in Low-Z	t _{CLZ}	3		ns	3
Output buffer turn-off delay from CAS	t _{CEZ}	3	15	ns	6,12
Transition time(rise and fall)	t _T	2	50	ns	2
RAS precharge time	t _{RP}	40		ns	
RAS pulse width	t _{RAS}	60	10K	ns	
RAS hold time	t _{RSH}	17		ns	
CAS hold time	t _{CSH}	50		ns	
CAS pulse width	t _{CAS}	10	10K	ns	4
RAS to CAS delay time	t _{RCD}	20	45	ns	9
RAS to column address delay time	t _{RAD}	15	30	ns	
CAS to RAS precharge time	t _{CRP}	5		ns	
Row address set-up time	t _{ASR}	0		ns	
Row address hold time	t _{RAH}	10		ns	
Column address set-up time	t _{ASC}	0		ns	
Column address hold time	t _{CAH}	10		ns	
Column address to RAS lead time	t _{RAL}	30		ns	
Read command set-up time	t _{RCS}	0		ns	
Read command hold referenced to CAS	t _{RCH}	0		ns	8
Read command hold referenced to RAS	t _{RRH}	0		ns	8
Write command set-up time	t _{WCS}	0		ns	7
Write command hold time	t _{WCH}	10		ns	
Write command pulse width	t _{WP}	10		ns	
Write command to RAS lead time	t _{RWL}	15		ns	
Write command to CAS lead time	t _{CWL}	10		ns	
Data set-up time	t _{DS}	0		ns	9
Data hold time	t _{DH}	10		ns	9
Refresh period (1K Ref)	t _{REF}	128		ms	
CAS setup time (CAS-before-RAS refresh)	t _{CSR}	5		ns	
CAS hold time (CAS-before-RAS refresh)	t _{CHR}	10		ns	
RAS to CAS precharge time	t _{RPC}	5		ns	
Access time from CAS precharge	t _{CPA}	20		ns	3

AC CHARACTERISTICS (continued)

Parameter	Symbol	60 nS		Unit	Note
		Min	Max		
Hyper page mode cycle time	tHPC	30		ns	11
CAS precharge time (Hyper page cycle)	tCP	10		ns	
Access time from CAS (Hyper page cycle)	tCACP		15		
Access time from col. Address (Hyper page cycle)	tAAP		30		
RAS pulse width (Hyper page cycle)	tRASP	60	200K	ns	
RAS hold time from CAS precharge	tRHCP	35		ns	
W to RAS precharge time(C-B-R refresh)	tWRP	10		ns	
W to RAS hold time(C-B-R refresh)	tWRH	10		ns	
Output data hold time	tDOH	5		ns	
Output buffer turn off delay from RAS	tREZ	3	15	ns	6,12
Output buffer turn off delay from W	tWEZ	3	15	ns	6
W to data delay	tWED	15		ns	
W pulse width	tWPE	5		ns	

NOTES

- An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
- Input voltage levels are V_{IH}/V_{IL} . $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
- Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
- This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL} .
- t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- These parameters are referenced to the CAS leading edge in early write cycles.
- Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit access time is controlled by t_{AA} .
- $t_{ASC} \geq 6ns$, Assume $t_T = 2.0ns$.
- If RAS goes high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes high before RAS high going, the open circuit condition of the output is achieved by RAS going.



NOTE: All dimensions in mm (mils).

All information in this data sheet is considered final, however, Memory Ten reserves the right to make changes as necessary.