

MemoryTen

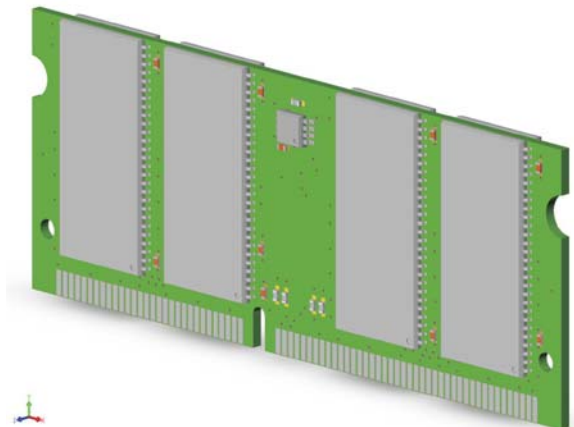
64S8S88-75LP 8 Meg X 64 SDRAM 144 Pin SO DIMM PC-133
 128S8S168-75LP 16 Meg X 64 SDRAM 144 Pin SO DIMM PC-133
 256S8S328-75LP 32 Meg X 64 SDRAM 144 Pin SO DIMM PC-133
 512S8S648-75LP 64 Meg X 64 SDRAM 144 Pin SO DIMM PC-133

Features

- PC133-compliant, 144-pin, small outline, Dual in-line memory module (SODIMM)
- Utilizes 143 MHz SDRAM components
- Unbuffered
- 64MB (8 Meg x 64), 128MB (16 Meg x 64), and 256MB (32 Meg x 64), 512MB (64 Meg x 64)
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/ precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode: Standard and Low Power
- 64MB and 128MB: 64ms, 4,096-cycle (15.625 μ s) refresh interval; 256MB and 512MB: 64ms, 8,192-cycle (7.8125 μ s) refresh interval
- LVTTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)
- Gold edge contacts

144-Pin SODIMM (MO-190)

1.035" tall



	64MB	128MB	256MB	512MB
Refresh Count	4K	4K	8K	8K
Device Banks	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)	4(BA0,BA1)
Device Configuration	64Mb (8 Meg x 8)	128Mb (16 Meg x 8)	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)
Row Addressing	4K (A0-A11)	4K (A0-A11)	8K (A0-A12)	8K(A0-A12)
Column Addressing	512 (A0-A8)	1024 (A0-A9)	1024 (A0-A9)	2048(A0-A9,A11)
Module Ranks	1 (S0#)	1 (S0#)	1 (S0#)	1 (S0#)

PRODUCTION DATA information is current as of publication date.
 Products conform to specifications per the terms of MemoryTen
 standard warranty. Production processing does not necessarily include
 testing of all parameters.

128S8S168-75LP.PDF
 REV A
 11-30-07

ALL SPECIFICATIONS FOR PRODUCTS DISCUSSED HEREIN ARE SUBJECT TO CHANGE BY MemoryTen WITHOUT NOTICE.

ORDERING INFORMATION

PART NUMBER	MODULE DENSITY	CONFIGURATION	SYSTEM BUS SPEED
64S8S88-75LP	64MB	8 Meg x 64	133 MHz
128S8S168-75LP	128MB	16 Meg x 64	133 MHz
256S8S328-75LP	256MB	32 Meg x 64	133 MHz
512S8S648-75LP	512MB	64 Meg x 64	133 MHz

Pin Assignment (144-Pin SODIMM Front)

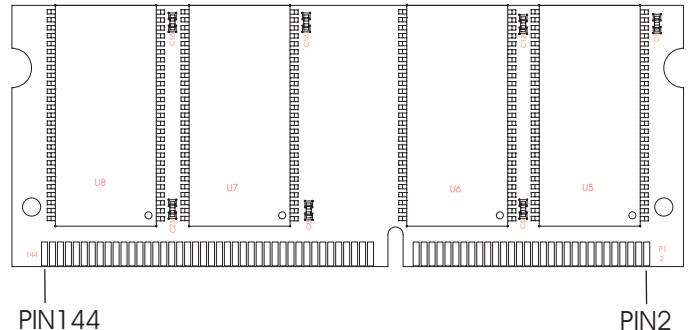
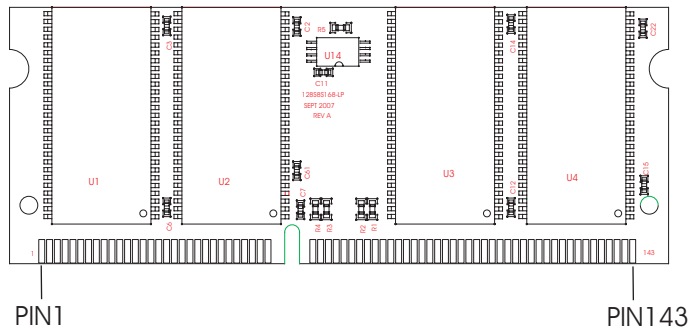
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	37	DQ8	73	NC	109	A9
3	DQ0	39	DQ9	75	Vss	111	A10
5	DQ1	41	DQ10	77	DNU	113	Vdd
7	DQ2	43	DQ11	79	DNU	115	DQMB2
9	DQ3	45	Vdd	81	Vdd	117	DQMB3
11	Vdd	47	DQ12	83	DQ16	119	Vss
13	DQ4	49	DQ13	85	DQ17	121	DQ24
15	DQ5	51	DQ14	87	DQ18	123	DQ25
17	DQ6	53	DQ15	89	DQ19	125	DQ26
19	DQ7	55	Vss	91	Vss	127	DQ27
21	Vss	57	DNU	93	DQ20	129	Vdd
23	DQMB0	59	DNU	95	DQ21	131	DQ28
25	DQMB1	61	CK0	97	DQ22	133	DQ29
27	Vdd	63	Vdd	99	DQ23	135	DQ30
29	A0	65	RAS#	101	Vdd	137	DQ31
31	A1	67	WE#	103	A6	139	Vss
33	A2	69	SO#	105	A8	141	SDA
35	Vss	71	S1#	107	Vss	143	Vdd

Pin Assignment (144-Pin SODIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
2	Vss	38	DQ40	74	CK1	110	BA1
4	DQ32	40	DQ41	76	Vss	112	A11
6	DQ33	42	DQ42	78	DNU	114	Vdd
8	DQ34	44	DQ43	80	DNU	116	DQMB6
10	DQ35	46	Vdd	82	Vdd	118	DQMB7
12	Vdd	48	DQ44	84	DQ48	120	Vss
14	DQ36	50	DQ45	86	DQ49	122	DQ56
16	DQ37	52	DQ46	88	DQ50	124	DQ57
18	DQ38	54	DQ47	90	DQ51	126	DQ58
20	DQ39	56	Vss	92	Vss	128	DQ59
22	Vss	58	DNU	94	DQ52	130	Vdd
24	DQMB4	60	DNU	96	DQ53	132	DQ60
26	DQMB5	62	CKE0	98	DQ54	134	DQ61
28	Vdd	64	Vdd	100	DQ55	136	DQ62
30	A3	66	CAS#	102	Vdd	138	DQ63
32	A4	68	CKE1	104	A7	140	Vss
34	A5	70	NC/A12 ¹	106	BA0	142	SCL
36	Vss	72	DNU	108	Vss	144	Vdd

NOTE:

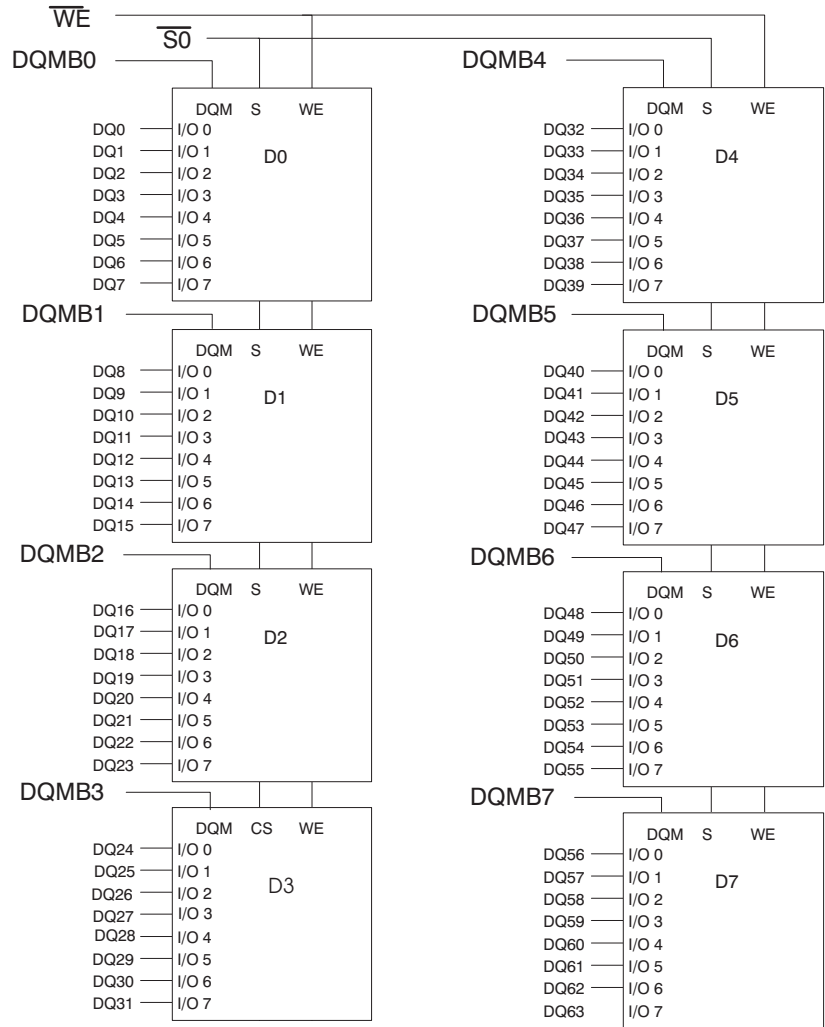
1. Pin 70 is No Connect for 64 MB and 128 MB modules, or is A12 for 256MB and 512MB modules.



Pin Descriptions

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
65, 66, 67	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
61, 74	CK0, CK1	Input	Clock: CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
62, 68	CKE0, CKE1	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. Deactivating the clock provides PRECHARGE, POWER-DOWN, and SELF REFRESH operation (all device banks idle), ACTIVE POWER-DOWN (row ACTIVE in any device bank), or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power.
69, 71	S0#, S1#	Input	Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
23, 24, 25, 26, 115, 116, 117, 118	DQMB0–DQMB7	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
106, 110	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
29, 30, 31, 32, 33, 34, 70 (256MB), 103, 104, 105, 109, 111, 112	A0–A11 (64MB, 128MB) A0–A12 (256MB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). Address inputs also provide the op-code during a MODE REGISTER SET command.
142	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
141	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
3–10, 13–20, 37–44, 47–54, 83–90, 93–100, 121–128, 131–138	DQ0–DQ63	Input/Output	Data I/O: Data bus.
11, 12, 27, 28, 45, 46, 63, 64, 81, 82, 101, 102, 113, 114, 129, 130, 143, 144	V _{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 2, 21, 22, 35, 36, 55, 56, 75, 76, 91, 92, 107, 108, 119, 120, 139, 140	V _{SS}	Supply	Ground.
70 (64MB, 128MB), 73	NC	–	Not Connected: These pins should be left unconnected.
57, 58, 59, 60, 72, 77, 78, 79, 80	DNU	–	Do Not Use: These pins are not connected on these modules, but are assigned pins on other modules in this product family.

Block Diagram



NOTE: All DQ lines have 10 ohm series damping resistors.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	D0,D1,D4,D5
*CK1	D2,D3,D6,D7

BA0 - BAN → BA0-BAN: SDRAMs D0 - D7

A0 - AN → A0-AN: SDRAMs D0 - D7

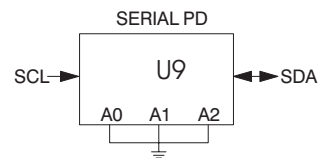
VDD → D0 - D7

VSS → D0 - D7

RAS → RAS: SDRAMs D0 - D7

CAS → CAS: SDRAMs D0 - D7

CKE0 → CKE: SDRAMs D0 - D7



Module Characteristics

DC Characteristics

$T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{DD}, V_{DDQ} = 3.3$ V \pm 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	$V_{CC}+0.3$	V
Input low voltage	V_{IL}	- 0.5	0.8	V
Output high voltage ($I_{OUT} = - 2.0$ mA)	V_{OH}	2.4	-	V
Output low voltage ($I_{OUT} = 2.0$ mA)	V_{OL}	-	0.4	V
Input leakage current, any input (0 V $< V_{IN} < 3.6$ V, all other inputs = 0 V)	$I_{I(L)}$	- 40	40	uA
Output leakage current (DQ is disabled, 0 V $< V_{OUT} < V_{CC}$)	$I_{O(L)}$	- 40	40	uA

Capacitance

$T_A = 0$ to 70 °C; $V_{DD} = 3.3$ V \pm 0.3 V, $f = 1$ MHz

Parameter	Symbol	Limit Values (max.)	Unit
Input capacitance (A0 to A10, BA, RAS, CAS, WE)	C_{I1}	80	pF
Input capacitance (CS0 -CS3)	C_{I2}	30	pF
Input capacitance (CLK0 - CLK3)	C_{ICL}	22	pF
Input capacitance (CKE0, CKE1)	C_{I3}	50	pF
Input capacitance (DQMB0 - DQMB7)	C_{I4}	20	pF
Input / Output capacitance (DQ0-DQ63)	C_{IO}	20	pF
Input Capacitance (SCL,SA0-2)	C_{Sc}	8	pF
Input/Output Capacitance	C_{Sd}	10	pF

IDD SPECIFICATIONS

Standby and Refresh Currents ($T_a = 0$ to 70°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

PARAMETER/CONDITION		SYMBOL	64 Mb	128Mb	256Mb	512Mb	UNITS
Operating Current: Active Mode; Burst = 2; READ or WRITE; $t_{RC} = t_{RC}(\text{MIN})$		IDD1	1000	1280	1080	960	mA
Standby Current: Power-Down Mode; CKE = LOW; All banks idle		IDD2	16	16	16	28	mA
Standby Current: Active Mode; CS# = HIGH; CKE = HIGH; All banks active after t_{RCD} met; No accesses in progress		IDD3	360	400	320	360	mA
Operating Current: Burst Mode; Page burst; READ or WRITE; All banks active		IDD4	1200	1320	1080	920	mA
Auto Refresh Current: CS# = HIGH; CKE = HIGH	$t_{RFC} = t_{RFC}(\text{MIN})$	IDD5	1840	2640	2280	1000	mA
	$t_{RFC} = 7.81\mu\text{s}$	IDD6	24	24	28	48	mA
Self Refresh Current: CKE ? 0.2V	Standard	IDD7	8	16	20	48	mA

AC CHARACTERISTICS

T_A=0 to 70°C, V_{SS}=0V, V_{CC}=3.3V±0.3V, t=1ns

Parameter	Symbol	Limit Values		Unit
		-75 PC133 2-2-2		
		Min.	Max.	
Clock and Clock Enable				
Clock Cycle Time CAS Latency = 3 CAS Latency = 2	t_{CK}			
		7.7		ns
		7		ns
System Frequency CAS Latency = 3 CAS Latency = 2	f_{CK}			
		–	133	MHz
		–	133	MHz
Clock Access Time CAS Latency = 3 CAS Latency = 2	t_{AC}			
		–	5.4	ns
		–	5.4	ns
Clock High Pulse Width	t_{CH}	2.5	–	ns
Clock Low Pulse Width	t_{CL}	2.5	–	ns
Input Setup time	t_{CS}	1.5	–	ns
Input Hold time	t_{CH}	.8	–	ns
CKE Setup Time (Power Down Mode)	t_{CKSP}	1.5	–	ns
CKE Setup Time (Self Refresh Mode)	t_{CKSR}	6	–	ns
Transition Time (rise and fall)	t_T	1	–	ns
Common Parameters				
RAS to CAS delay	t_{RCD}	15	–	ns
Cycle Time	t_{RC}	60	120k	ns
Active Command Period	t_{RAS}	37	–	ns
Precharge Time	t_{RP}	15	–	ns
Bank to Bank Delay Time	t_{RRD}	16	–	ns
CAS to CAS delay time (same bank)	t_{CCD}	1	–	CLK

AC CHARACTERISTICS CONTINUED

Parameter	Symbol	Limit Values		Unit
		-75 PC133 2-2-2		
		Min.	Max.	
Refresh Cycle				
Self Refresh Exit Time	t_{SREX}	10	–	ns
Refresh Period (4096 cycles)	t_{REF}	64	–	ms
Refresh Period (8192 cycles)	t_{REF}	64	–	ms
Read Cycle				
Data Out Hold Time	t_{OH}	2.7	–	ns
Data Out to Low Impedance Time	t_{LZ}	1	–	ns
Data Out to High Impedance Time	t_{HZ}	3	9	ns
DQM Data Out Disable Latency	t_{DQZ}	2	–	CLK
Write Cycle				
Data input to Precharge(write Recovery)	t_{DPL}	2	–	CLK
Data In to Active/refresh	t_{DAL}	2	–	CLK
DQM Write Mask Latency	t_{DQW}	0	–	CLK

Notes:

1. The specified values are valid when addresses are changed no more than once during $t_{CK}(\text{min.})$ and when No Operation commands are registered on every rising clock edge during $t_{RC}(\text{min.})$. Values are shown per module bank.
2. The specified values are valid when data inputs (DQs) are stable during $t_{RC}(\text{min.})$.
3. All AC characteristics are shown for device level.
An initial pause of 100ns is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have $V_{il} = 0.4 \text{ V}$ and $V_{ih} = 2.4 \text{ V}$ with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il} . All AC measurements assume $t_T = 1 \text{ ns}$ with the AC output load circuit show. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.

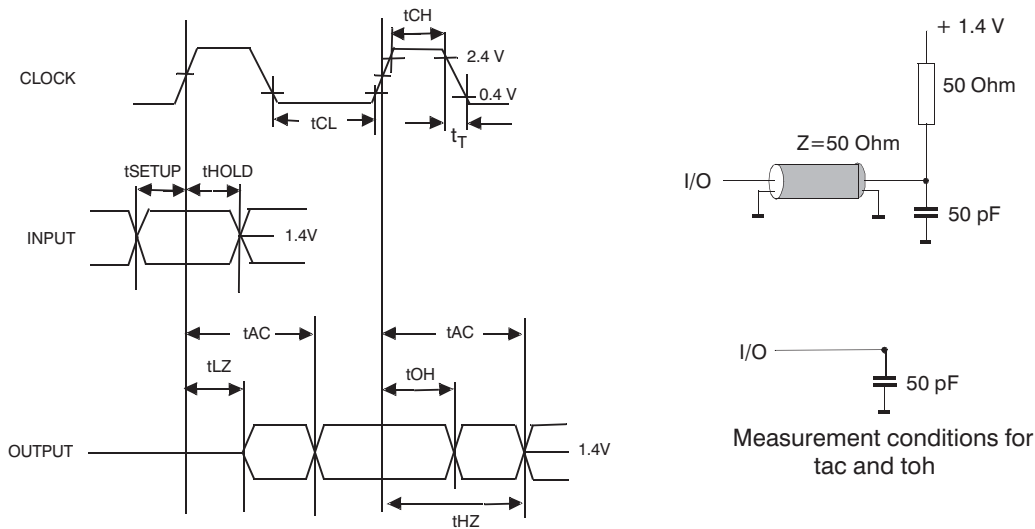


fig.1

5. If clock rising time is longer than 1ns, a time $(t_T/2 - 0.5) \text{ ns}$ has to be added to this parameter.
6. Rated at 1.5 V
7. If t_T is longer than 1 ns, a time $(t_T - 1) \text{ ns}$ has to be added to this parameter.
8. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
11. t_{DAL} is equivalent to $t_{DPL} + t_{RP}$.

Serial Presents Detect (SPD)

D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Units
I _{CCR}	Read Current	Read, f _{SCL} = 400kHz		1	mA
I _{CCW}	Write Current	Write, f _{SCL} = 400kHz		2	mA
I _{SB}	Standby Current	All I/O Pins at GND or V _{CC}	T _A = -40°C to +85°C	1	μA
			T _A = -40°C to +125°C	2	
I _L	I/O Pin Leakage	Pin at GND or V _{CC}	T _A = -40°C to +85°C	1	μA
			T _A = -40°C to +125°C	2	
V _{IL}	Input Low Voltage		-0.5	V _{CC} × 0.3	V
V _{IH}	Input High Voltage		V _{CC} × 0.7	V _{CC} + 0.5	V
V _{OL1}	Output Low Voltage	V _{CC} < 2.5 V, I _{OL} = 3.0mA		0.4	V
V _{OL2}	Output Low Voltage	V _{CC} < 2.5 V, I _{OL} = 1.0mA		0.2	V

PIN IMPEDANCE CHARACTERISTICS

--	Parameter	Conditions	Max	Units
C _{IN}	SDA I/O Pin Capacitance	V _{IN} = 0 V	8	pF
C _{IN}	Input Capacitance (other pins)	V _{IN} = 0 V	6	pF
I _{WP}	WP Input Current	V _{IN} < V _{IH} , V _{CC} = 5.5 V	200	μA
		V _{IN} < V _{IH} , V _{CC} = 3.3 V	150	
		V _{IN} < V _{IH} , V _{CC} = 1.8 V	100	
		V _{IN} > V _{IH}	1	

A.C. CHARACTERISTICS^①

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C.

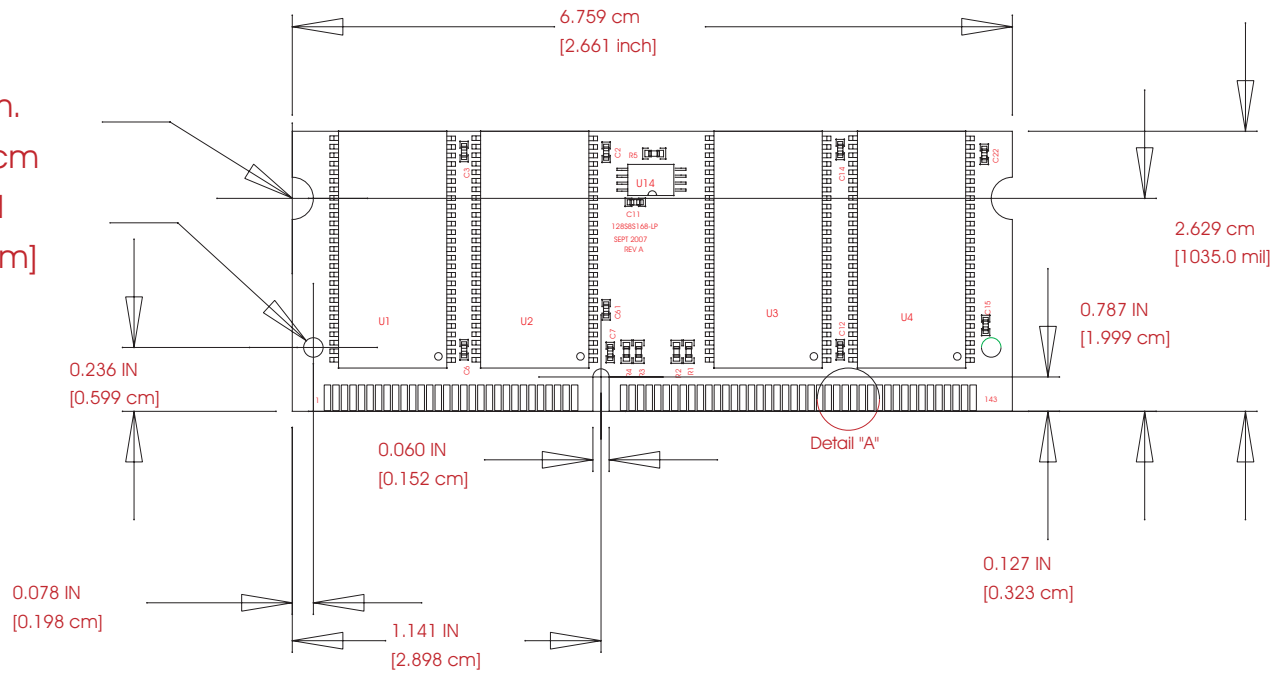
Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
SCL	Clock Frequency		100		400	kHz
t _{HD:STA}	START Condition Hold Time	4		0.6		μs
t _{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t _{HIGH}	High Period of SCL Clock	4		0.6		μs
t _{SU:STA}	START Condition Setup Time	4.7		0.6		μs
t _{HD:DAT}	Data In Hold Time	0		0		μs
t _{SU:DAT}	Data In Setup Time	250		100		ns
t _R	SDA and SCL Rise Time		1000		300	ns
t _F	SDA and SCL Fall Time		300		300	ns
t _{SU:STO}	STOP Condition Setup Time	4		0.6		μs
t _{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
t _{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t _{DH}	Data Out Hold Time	100		100		ns
T _i	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
t _{SU:WP}	WP Setup Time	0		0		μs
t _{HD:WP}	WP Hold Time	2.5		2.5		μs
t _{WR}	Write Cycle Time		5		5	ms
t _{PU}	Power-up to Ready Mode		1		1	ms

A.C. TEST CONDITIONS

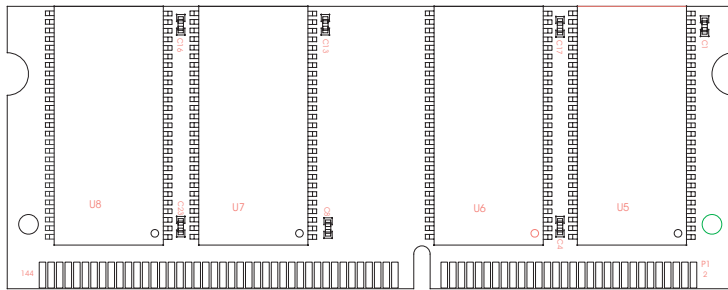
Input Levels	0.2 x V _{CC} to 0.8 x V _{CC}
Input Rise and Fall Times	≤50 ns
Input Reference Levels	0.3 x V _{CC} , 0.7 x V _{CC}
Output Reference Levels	0.5 x V _{CC}
Output Load	Current Source: I _{OL} = 3 mA (V _{CC} ≥ 2.5 V); I _{OL} = 1 mA (V _{CC} < 2.5 V); C _L = 100 pF

FRONT VIEW

R .078 in.
R 2.00 cm
0.072 IN
[0.183 cm]



BACK VIEW



(0.114)

(0.040)

NOTE: All dimensions in inches (cm).

All information in this data sheet is considered final, however, Memory Ten reserves the right to make changes as necessary.