

MemoryTen

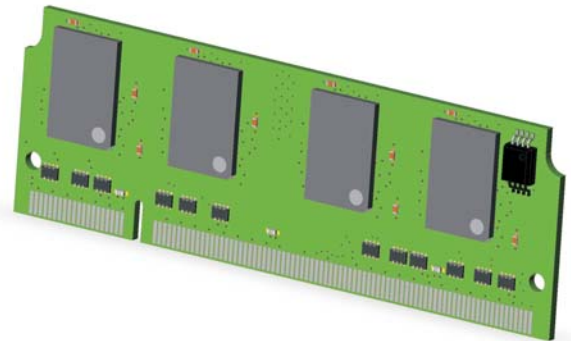
128S4D1616-32LP	16 Meg X 64	DDR1	200 Pin	SO DIMM	PC-3200
256S8D1616-32LP	32 Meg X 64	DDR1	200 Pin	SO DIMM	PC-3200
256S4D3216-32LP	32 Meg X 64	DDR1	200 Pin	SO DIMM	PC-3200
512S8D3216-32LP	64 Meg X 64	DDR1	200 Pin	SO DIMM	PC-3200

Features

- PC3200-compliant, 200-pin, smalloutline, Dual in-line memory module (SODIMM)
- Utilizes 400 (200MHZ CLK) MHZ DDR1 SDRAM components
- Unbuffered
- 128MB (16 Meg x 64), 256MB (32 Meg x 64), and 512MB (64 Meg x 64)
- Single +2.5V power supply
- VDDSPD = 2.5V TO 3.6v
- Differential Clock
- Internal pipelined double data rate operation; 2 data accesses per clock cycle.
- Multiple Internal SDRAM banks for concurrent access operation
- Bidirectional data strobe (DQS) source-synchronous data capture
- Programmable burst lengths: 1, 2, 4, or 8
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 128MB (15.625µs) refresh interval; 256MB, and 512MB: (7.8125µs) refresh interval
- 2.5v SSTTL_2 -compatible inputs and outputs
- Serial Presence-Detect (SPD)
- Gold edge contacts
- Selectable CAS latency

200-Pin SODIMM (MO-224B)

.9" tall



ADDRESSING

Parameter	128MB	256MB	512MB
Refresh count	8K	8K	8K
Row address	8K(A0-A12)	8K (A0-A12)	8K (A0-A12)
Device bank address	4(BA0-BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	128Mb (16 Meg X 16)	256Mb (16 Meg x 16)	512Mb (32 Meg x 16)
Column address	512 (A0-A8)	512 (A0-A8)	1K (A0-A9)
Module rank address	1 (S0#)	2 (S0#, S1#)	2 (S0#, S1#)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of MemoryTen standard warranty. Production processing does not necessarily include testing of all parameters.

MT512S8D3216-32LP.CDR
REV B
11-28-07

ALL SPECIFICATIONS FOR PRODUCTS DISCUSSED HEREIN ARE SUBJECT TO CHANGE BY MemoryTen WITHOUT NOTICE.

General Description

The 128S4D1616-32LP, 256S8D1616-32LP, and 512S8D3216-32LP are high-speed, CMOS, dynamic random access 128MB, 256MB, and 512MB memory modules organized in a x64 configuration. DDR SDRAM devices use internally configured, 4-bank (128Mb, 256Mb, or 512Mb) DDR SDRAM devices. DDR SDRAM modules transmit data on both the rising and falling edge of the clock (double data rate architecture) to achieve high-speed operation.

The double data rate architecture is a $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle on the I/O pins. A single read or write access for DDR SDRAM modules consist of a single $2n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n -bit-wide, one-half-clock-cycle data transfers to/from the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK.

Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Key Timing Parameters

Industry Nomenclature	Data Rate (MT/s)			tRCD (ns)	tRP (ns)	tRC (ns)
	CL = 3	CL = 2.5	CL = 2			
PC3200	400	333	266	15	15	55

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-tRCD-tRP)
128S4D1616-32LP	128MB	16 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
256S8D1616-32LP	256MB	32 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
512S8D3216-32LP	512MB	64 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Pin Assignment (200-Pin SODIMM Front)

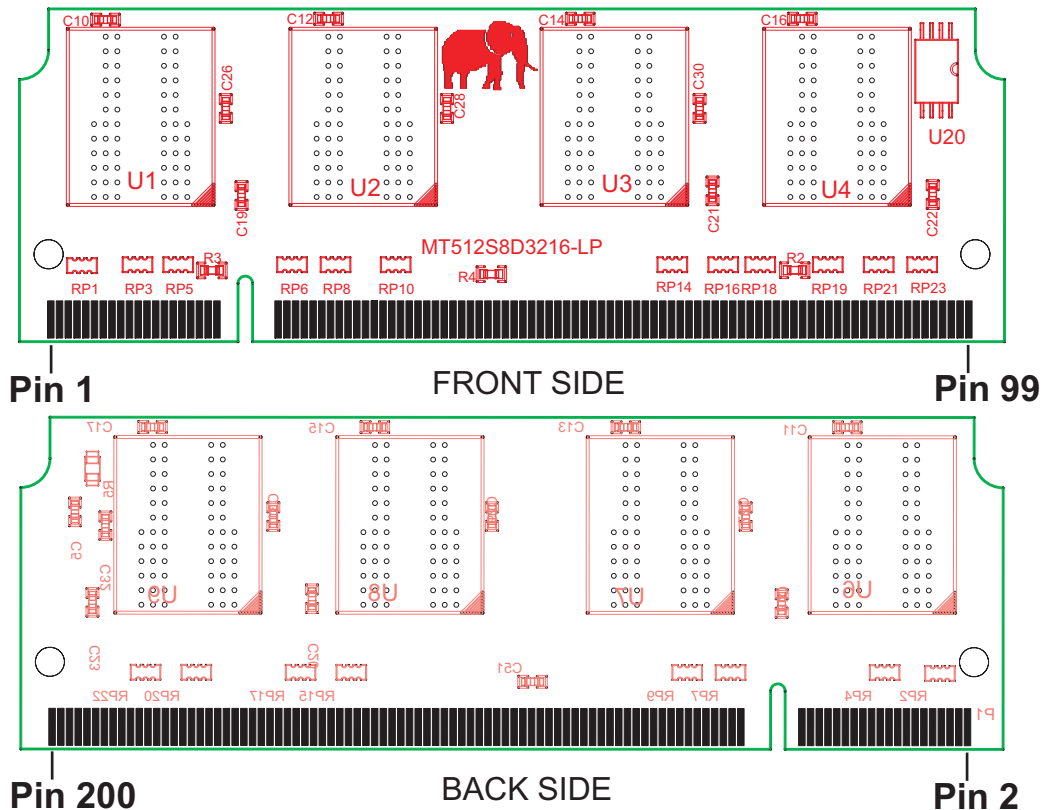
Pin Assignment (200-Pin SODIMM Back)

200-Pin SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	VSS	101	A9	151	DQ42
3	VSS	53	DQ19	103	VSS	153	DQ43
5	DQ0	55	DQ24	105	A7	155	VDD
7	DQ1	57	VDD	107	A5	157	VDD
9	VDD	59	DQ25	109	A3	159	VSS
11	DQS0	61	DQS3	111	A1	161	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48
15	VSS	65	DQ26	115	A10	165	DQ49
17	DQ3	67	DQ27	117	BA0	167	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6
21	VDD	71	NC	121	SO#	171	DQ50
23	DQ9	73	NC	123	NC/A13	173	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51
27	VSS	77	NC	127	DQ32	177	DQ56
29	DQ10	79	NC	129	DQ33	179	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57
33	VDD	83	NC	133	DQS4	183	DQS7
35	CK0	85	NC	135	DQ34	185	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58
39	VSS	89	NC	139	DQ35	189	DQ59
41	DQ16	91	NC	141	DQ40	191	VDD
43	DQ17	93	VDD	143	VDD	193	SDA
45	VDD	95	CKE1	145	DQ41	195	SCL
47	DQS2	97	NC	147	DQS5	197	VDDSPD
49	DQ18	99	NC/A12	149	VSS	199	NC

200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	VREF	52	VSS	102	A8	152	DQ46
4	VSS	54	DQ23	104	VSS	154	DQ47
6	DQ4	56	DQ28	106	A6	156	VDD
8	DQ5	58	VDD	108	A4	158	CK1#
10	VDD	60	DQ29	110	A2	160	CK1
12	DM0	62	DM3	112	A0	162	VSS
14	DQ6	64	VSS	114	VDD	164	DQ52
16	VSS	66	DQ30	116	BA1	166	DQ53
18	DQ7	68	DQ31	118	RAS#	168	VDD
20	DQ12	70	VDD	120	CAS#	170	DM6
22	VDD	72	NC	122	S1#	172	DQ54
24	DQ13	74	NC	124	NC	174	VSS
26	DM1	76	VSS	126	VSS	176	DQ55
28	VSS	78	NC	128	DQ36	178	DQ60
30	DQ14	80	NC	130	DQ37	180	VDD
32	DQ15	82	VDD	132	VDD	182	DQ61
34	VDD	84	NC	134	DM4	184	DM7
36	VDD	86	NC	136	DQ38	186	VSS
38	VSS	88	VSS	138	VSS	188	DQ62
40	VSS	90	VSS	140	DQ39	190	DQ63
42	DQ20	92	VDD	142	DQ44	192	VDD
44	DQ21	94	VDD	144	VDD	194	SA0
46	VDD	96	CKE0	146	DQ45	196	SA1
48	DM2	98	NC	148	DM5	198	SA2
50	DQ22	100	A11	150	VSS	200	NC

NOTE:

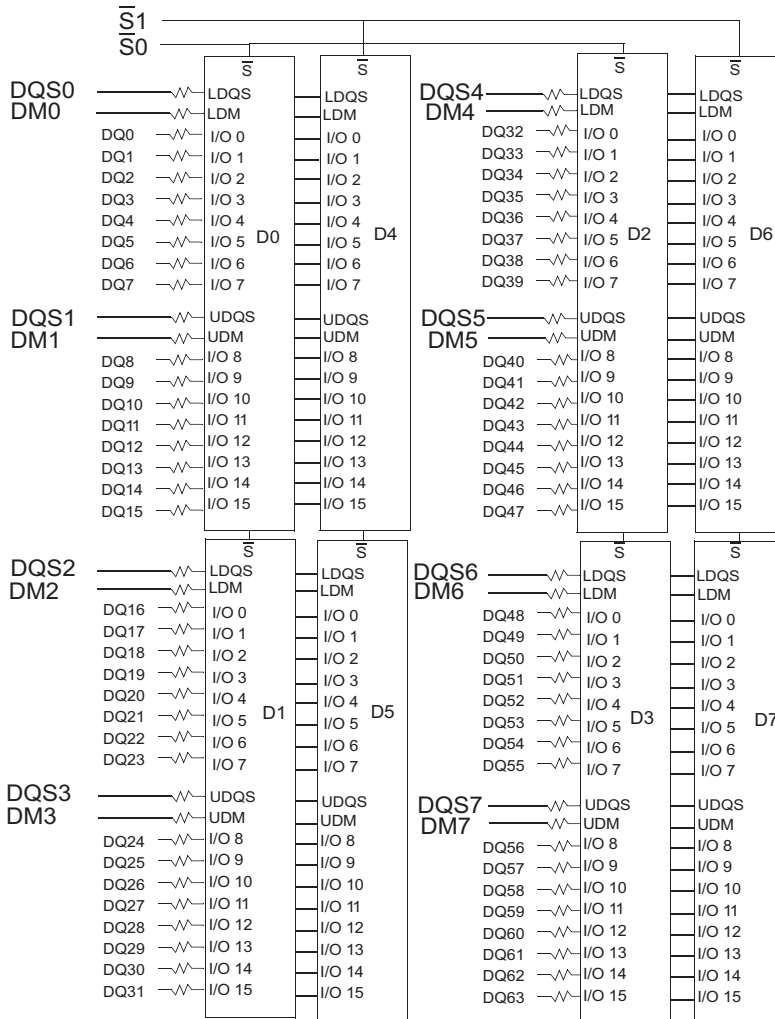
1. Pin 123 is No Connect for 128 MB, 256MB and 512 MB modules.



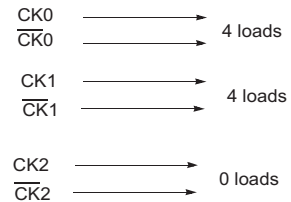
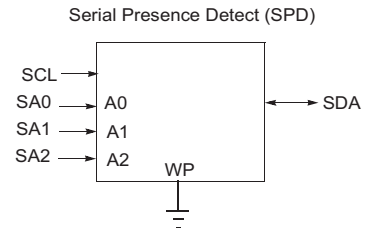
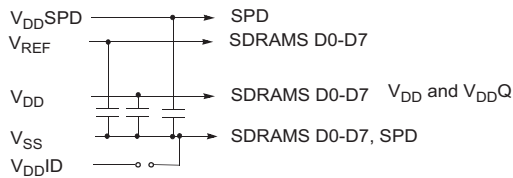
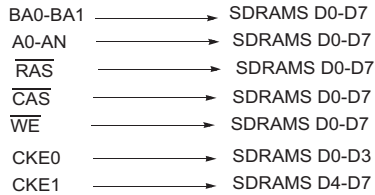
Pin Descriptions

Symbol	Type	Description
A0–A13	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. A0–A12 (128MB, 256MB, 512MB).
BA0, BA1	Input	Bank address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK0, CK0#, CK1, CK1#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE0, CEK1	Input	Clock enable: CEK HIGH activates and CEK LOW deactivates the internal clock, input buffers, and output drivers.
DM0–DM7	Input	Data write mask: DM LOW enables WRITE operation. DM HIGH blocks WRITE operation. DM lines do not affect READ operation.
S0#, S1#	Input	Chip selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
SA0–SA2	Input	Presence-detect address inputs: These pins are used to configure the presence-detect device.
SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
WE#, CAS#, RAS#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
DQ0–DQ63	I/O	Data I/Os: Data bus.
DQS0–DQS7	I/O	Data strobe: Output with read data; input with write data. DQS is edge-aligned with read data, center-aligned with write data. Used to capture data.
SDA	I/O	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
VDD	Supply	Power supply: +2.5V ±0.2V
VDDSPD	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
VREF	Supply	SSTL_2 reference voltage (VDD/2).
VSS	Supply	Ground.
NC	–	No connect: These pins are not connected on the module.

Block Diagram



#Unless otherwise noted, resistor values are $22 \Omega \pm 5\%$



Note: DQ wiring may differ from that described in this drawing; however DQ/DM/DQS relationships are maintained as shown.
 $V_{DD}ID$ strap connections:
 (for memory device V_{DD} , V_{DDQ})
 Strap out (open): $V_{DD} = V_{DDQ}$
 Strap in (closed): $V_{DD} \neq V_{DDQ}$

For 128S4D1616-21LP only D0, D1, D2, and D3 are installed.

Module Characteristics

Absolute Maximum Ratings

All voltages referenced to Vss.

Parameter	Absolute Maximum Value
VDDsupply voltage	-1V to +3.6V
VDDQ supply voltage	-1V to +3.6V
VREFand inputs voltage	-1V to +3.6V
I/O pins voltage	-0.5V to VDDQ +0.5V
Storage temperature (plastic)	-55°C to +150°C
Short circuit output current	50mA

DC Characteristics

TA = 0 to 70 °C; VSS = 0 V; VDD, VDDQ = 2.5 V ± 0.2 V

Parameter/Condition	Symbol	Min	Max	Units	
Supply voltage	VDD	+2.3	+2.7	V	
I/O supply voltage	VDDQ	+2.3	+2.7	V	
I/O reference voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	
I/O termination voltage (at the system level)	VTT	VREF- 0.04	VREF+ 0.04	V	
Input high (logic 1) voltage	VIH(DC)	VREF+ 0.15	VDD+ 0.3	V	
Input low (logic 0) voltage	VIL(DC)	-0.3	VREF- 0.15	V	
Input leakage current: Any input 0V ≤ VIN ≤ VDD, VREFpin 0V < VIN ≤ 1.35V (All other pins not under test = 0V)	II	-2	+2	µA	
Output leakage current: (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	-5	+5	µA	
Ambient operating temperatures	Commercial	TA	0	+70	°C

AC CHARACTERISTICS

AC operating conditions are given in the DDR component data sheets of the respective memory device manufacturer. The capacitance values in the following table are calculated values derived from typical values from the memory devices manufacturer's data sheets. The listed values do not take into account trace capacitance or trace inductance or trace length delays.

Capacitance

$T_A = 0$ to 70 $V_{DD} = 2.5\text{ V} - 0.2\text{ V}$, $f = 1\text{ MHz}$

Parameter	Symbol	128MB		256MB,512MB		Units
		Min	Max	Min	Max	
Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM	C _{IO}	3.5	4.5	7.0	9.0	pF
Input capacitance: Command and address	C _{I1}	14	18	28	36	pF
Input capacitance: CK, CK#	C _{I2}	6	10	6	10	pF
Input capacitance: CKE	C _{I3}	6.0	10	6.0	10	pF

I_{DD} SPECIFICATIONS

Standby and Refresh Currents (T_a = 0 to 70°C, V_{CC} = 2.6V ± 0.2V)

Parameter/Condition	Symbol	128MB	256MB	512MB,	Units	
Operating one bank active-precharge current: t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	IDD01	512	556	640	mA	
Operating one bank active-read-precharge current: BL = 4; t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	IDD11	552	756	800	mA	
Precharge power-down standby current: All device banks idle; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = LOW	IDD2P2	24	32	40	mA	
Idle standby current: CS# = HIGH; All device banks idle; t _{CK} = t _{CK} (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ, DQS, and DM	IDD2F2	400	480	440	mA	
Active power-down standby current: One device bank active; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = LOW	IDD3P2	200	320	360	mA	
Active standby current: CS# = HIGH; CKE = HIGH; One device bank; Active precharge; t _{RC} = t _{RAS} (MAX); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N2	400	560	480	mA	
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA	IDD4R1	752	1,056	860	mA	
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W1	732	876	880	mA	
Auto refresh current	t _{REFC} = t _{RFC} (MIN)	IDD52	2,120	2,080	2,760	mA
	t _{REFC} = 15.625μs	IDD5A2	80	48	88	mA
Self refresh current: CKE ≤ 0.2V	IDD62	32	32	48	mA	
Operating bank interleave read current: Four device bank interleaving reads; BL = 4 with auto precharge; t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); Address and control inputs change only during active READ or WRITE commands	IDD71	1,552	2,056	1,940	mA	

Serial Presents Detect (SPD)

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit nonvolatile EEPROM configured as 2 blocks of 128 X 8 bits. The first 128 bytes are programmed by Memory Ten to identify the module type, SDRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device on the DIMM occur via a standard I2C bus using the DIMM's SCL (clock) and SDA (data) signals. SA0 - SA2) provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to VSS on the module, permanently disabling hardware write protect.

D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Units
I _{CCR}	Read Current	Read, f _{SCL} = 400kHz		1	mA
I _{CCW}	Write Current	Write, f _{SCL} = 400kHz		2	mA
I _{SB}	Standby Current	All I/O Pins at GND or V _{CC}	T _A = -40°C to +85°C	1	μA
			T _A = -40°C to +125°C	2	
I _L	I/O Pin Leakage	Pin at GND or V _{CC}	T _A = -40°C to +85°C	1	μA
			T _A = -40°C to +125°C	2	
V _{IL}	Input Low Voltage		-0.5	V _{CC} x 0.3	V
V _{IH}	Input High Voltage		V _{CC} x 0.7	V _{CC} + 0.5	V
V _{OL1}	Output Low Voltage	V _{CC} < 2.5 V, I _{OL} = 3.0mA		0.4	V
V _{OL2}	Output Low Voltage	V _{CC} < 2.5 V, I _{OL} = 1.0mA		0.2	V

PIN IMPEDANCE CHARACTERISTICS

--	Parameter	Conditions	Max	Units
C _{IN}	SDA I/O Pin Capacitance	V _{IN} = 0 V	8	pF
C _{IN}	Input Capacitance (other pins)	V _{IN} = 0 V	6	pF
I _{WP}	WP Input Current	V _{IN} < V _{IH} , V _{CC} = 5.5 V	200	μA
		V _{IN} < V _{IH} , V _{CC} = 3.3 V	150	
		V _{IN} < V _{IH} , V _{CC} = 1.8 V	100	
		V _{IN} > V _{IH}	1	

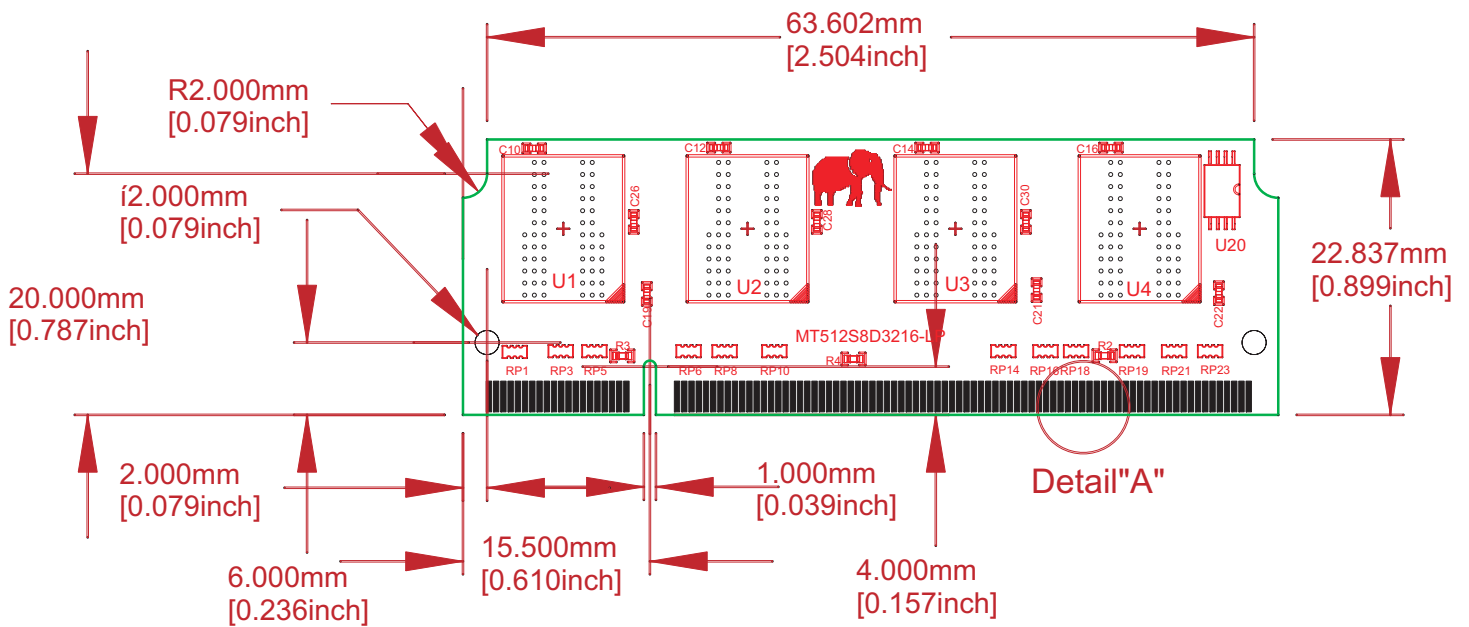
A.C. CHARACTERISTICS^①V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C.

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
SCL	Clock Frequency		100		400	kHz
t _{HD:STA}	START Condition Hold Time	4		0.6		μs
t _{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t _{HIGH}	High Period of SCL Clock	4		0.6		μs
t _{SU:STA}	START Condition Setup Time	4.7		0.6		μs
t _{HD:DAT}	Data In Hold Time	0		0		μs
t _{SU:DAT}	Data In Setup Time	250		100		ns
t _R	SDA and SCL Rise Time		1000		300	ns
t _F	SDA and SCL Fall Time		300		300	ns
t _{SU:STO}	STOP Condition Setup Time	4		0.6		μs
t _{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
t _{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t _{DH}	Data Out Hold Time	100		100		ns
T _i	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
t _{SU:WP}	WP Setup Time	0		0		μs
t _{HD:WP}	WP Hold Time	2.5		2.5		μs
t _{WR}	Write Cycle Time		5		5	ms
t _{PU}	Power-up to Ready Mode		1		1	ms

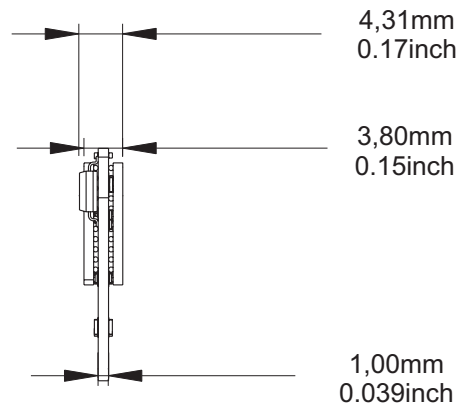
A.C. TEST CONDITIONS

Input Levels	0.2 x V _{CC} to 0.8 x V _{CC}
Input Rise and Fall Times	≤50 ns
Input Reference Levels	0.3 x V _{CC} , 0.7 x V _{CC}
Output Reference Levels	0.5 x V _{CC}
Output Load	Current Source: I _{OL} = 3 mA (V _{CC} ≥ 2.5 V); I _{OL} = 1 mA (V _{CC} < 2.5 V); C _L = 100 pF

FRONT VIEW



END VIEW



NOTES:

1. All dimensions in mm[inches].
2. The above diagram is for reference only. Refer to JEDEC MO document for additional dimensions.

All information in this data sheet is considered final, however, Memory Ten reserves the right to make changes as necessary.