

MemoryTen

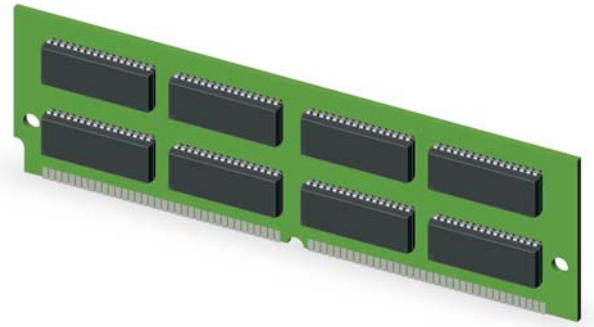
64T8E644-60 16Meg X 32 EDO 72 Pin Simm

Features

- JEDEC standard 72 pin Single Inline Memory Module (SIMM),
- JEDEC standard PDPin & Pinout
- 64MB (16 Meg x 32), single bank
- 128MB (32 Meg x 32), double bank
- Single 5V power supply
- Extended Data Output (EDO) mode operation
- CAS* - before - RAS* (CBR) & hidden refresh capable
- RAS* Only refresh capable
- 64MB and 128MB: 64ms, 4,096-cycle (15.625 μ s) refresh interval
- TTL-compatible inputs and outputs
- PCB: Height (1253mil), double sided component
- PCB: Tin-lead fingers standard

72-Pin SIMM (MO-116b)

1.253" tall



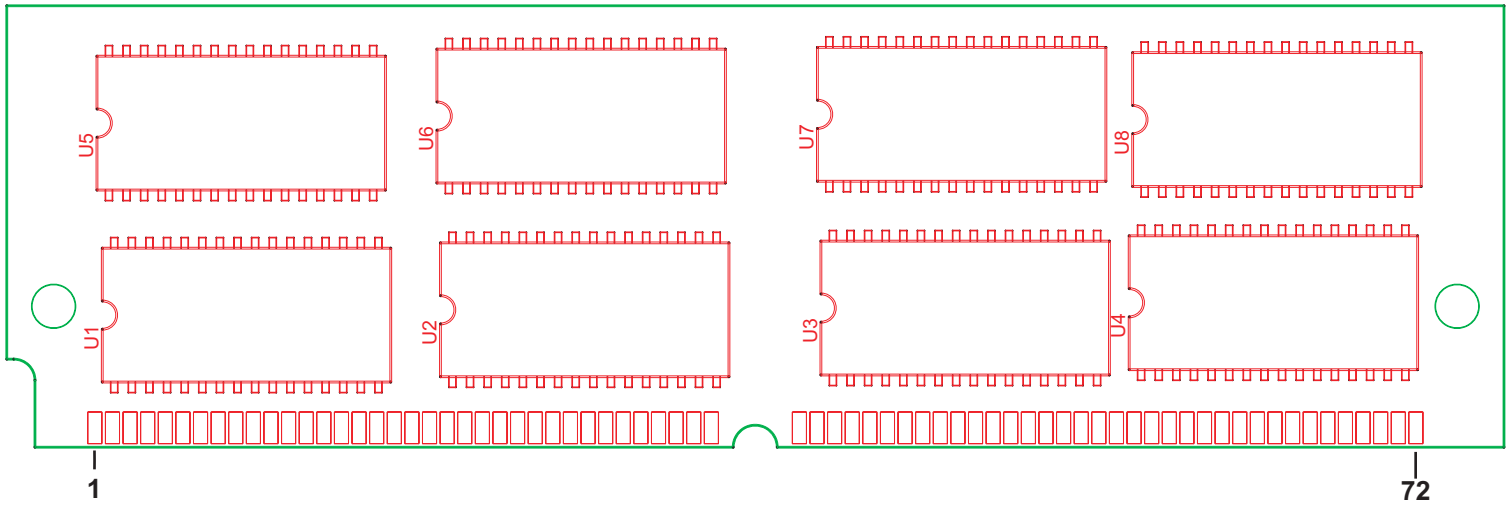
Representative assembly

ORDERING INFORMATION
72 Pin 5volt EDO, 1 bank SIMM, 64MB

| Part Number | Density | Speed | Chip Part Number | | Module Config | Chip Density | Brand |
|-------------------|---------|-------|---|------|---------------|--------------|----------|
| 64T8E64-60-SAM5 | 64MB | 60 ns | KM44C16104AK-6/BK-6/CK-6 | SOJ | 16Mx32 | 16Mx4 | Samsung |
| 64T8E644-60-MIC | 64MB | 60 ns | MT4LC16M4H9DJ-6 | SOJ | 16Mx32 | 16Mx4 | Micron |
| 64T8E644-60-HYN | 64MB | 60 ns | HY51V65403HG-60 | SOJ | 16Mx32 | 16Mx4 | Hynix |
| 64T8E644-60-SAM | 64MB | 60 ns | KM44V16104AK-6/BK-6/CK-6 | SOJ | 16Mx32 | 16Mx4 | Samsung |
| 64T8E644-60-GS | 64MB | 60 ns | GM71V65403CJ-6 | SOJ | 16Mx32 | 16Mx4 | Goldstar |
| 64T8E644-60-T | 64MB | 60 ns | unspecified | TSOP | 16Mx32 | 16Mx4 | Samsung |
| 64T8E644-60-MIC-T | 64MB | 60 ns | MT4LC16M4H9TG-6 | TSOP | 16Mx32 | 16Mx4 | Micron |
| 64T8E644-60-HYN-T | 64MB | 60 ns | HY51V65404ATC-60 | TSOP | 16Mx32 | 16Mx4 | Hynix |
| 64T8E644-60-SAM-T | 64MB | 60 ns | KM44V16104AS-6/BS-6/CS-6 | TSOP | 16Mx32 | 16Mx4 | Samsung |
| 64T8E644-60-GS-T | 64MB | 60 ns | GM71V64403CT6 | TSOP | 16Mx32 | 16Mx4 | Goldstar |
| 64T8E644-50 | 64MB | 50 ns | unspecified | SOJ | 16Mx32 | | Samsung |
| 64T8E644-50-MIC | 64MB | 50 ns | MT4LC16M4H9DJ-5 | SOJ | 16Mx32 | 16Mx4 | Micron |
| 64T8E644-50-HYN | 64MB | 50 ns | HY51V65404ATC-50 | SOJ | 16Mx32 | 16Mx4 | Hynix |
| 64T8E644-50-SAM | 64MB | 50 ns | KM44V16104AK-5/BK-5/CK-5, K4E640412D-JC50 | SOJ | 16Mx32 | 16Mx4 | Samsung |
| 64T8E644-50-GS | 64MB | 50 ns | GM71V65403CJ-5 | SOJ | 16Mx32 | 16Mx4 | Goldstar |
| 64T8E644-50-T | 64MB | 50 ns | unspecified | TSOP | 16Mx32 | 16Mx4 | Samsung |
| 64T8E644-50-MIC-T | 64MB | 50 ns | MT4LC16M4H9TG-5 | TSOP | 16Mx32 | 16Mx4 | Micron |
| 64T8E644-50-HYN-T | 64MB | 50 ns | HY51V6540ATC-50 | TSOP | 16Mx32 | 16Mx4 | Hynix |
| 64T8E644-50-SAM-T | 64MB | 50 ns | KM44V16104AS-5/BS-5/CS-5 | TSOP | 16Mx32 | 16Mx4 | Samsung |
| 64T8E644-50-GS-T | 64MB | 50 ns | GM71V64403CT5 | TSOP | 16Mx32 | 16Mx4 | Goldstar |

ORDERING INFORMATION
72 Pin 5volt EDO, 2 bank SIMM, 128MB

| Part Number | Density | Speed | Chip Part Number | | Module Config | Chip Density | Brand |
|---------------------|---------|-------|---|------|---------------|--------------|----------|
| 128T16E64-60SAM5 | 128MB | 60 ns | KM44C16104AK-6/BK-6/CK-6 | SOJ | 32Mx32 | 16Mx4 | Samsung |
| 128T16E644-60-MIC | 128MB | 60 ns | MT4LC16M4H9DJ-6 | SOJ | 32Mx32 | 16Mx4 | Micron |
| 128T16E644-60-HYN | 128MB | 60 ns | HY51V65403HG-60 | SOJ | 32Mx32 | 16Mx4 | Hynix |
| 128T16E644-60-SAM | 128MB | 60 ns | KM44V16104AK-6/BK-6/CK-6 | SOJ | 32Mx32 | 16Mx4 | Samsung |
| 128T16E644-60-GS | 128MB | 60 ns | GM71V65403CJ-6 | SOJ | 32Mx32 | 16Mx4 | Goldstar |
| 128T16E644-60-T | 128MB | 60 ns | unspecified | TSOP | 32Mx32 | 16Mx4 | Samsung |
| 128T16E644-60-MIC-T | 128MB | 60 ns | MT4LC16M4H9TG-6 | TSOP | 32Mx32 | 16Mx4 | Micron |
| 128T16E644-60-HYN-T | 128MB | 60 ns | HY51V65404ATC-60 | TSOP | 32Mx32 | 16Mx4 | Hynix |
| 128T16E644-60-SAM-T | 128MB | 60 ns | KM44V16104AS-6/BS-6/CS-6 | TSOP | 32Mx32 | 16Mx4 | Samsung |
| 128T16E644-60-GS-T | 128MB | 60 ns | GM71V64403CT6 | TSOP | 32Mx32 | 16Mx4 | Goldstar |
| 128T16E644-50 | 128MB | 50 ns | unspecified | SOJ | 32Mx32 | 16Mx4 | Samsung |
| 128T16E644-50-MIC | 128MB | 50 ns | MT4LC16M4H9DJ-5 | SOJ | 32Mx32 | 16Mx4 | Micron |
| 128T16E644-50-HYN | 128MB | 50 ns | HY51V65404ATC-50 | SOJ | 32Mx32 | 16Mx4 | Hynix |
| 128T16E644-50-SAM | 128MB | 50 ns | KM44V16104AK-5/BK-5/CK-5, K4E640412D-JC50 | SOJ | 32Mx32 | 16Mx4 | Samsung |
| 128T16E644-50-GS | 128MB | 50 ns | GM71V65403CJ-5 | SOJ | 32Mx32 | 16Mx4 | Goldstar |
| 128T16E644-50-T | 128MB | 50 ns | unspecified | TSOP | 32Mx32 | 16Mx4 | Samsung |
| 128T16E644-50-MIC-T | 128MB | 50 ns | MT4LC16M4H9TG-5 | TSOP | 32Mx32 | 16Mx4 | Micron |
| 128T16E644-50-HYN-T | 128MB | 50 ns | HY51V6540ATC-50 | TSOP | 32Mx32 | 16Mx4 | Hynix |
| 128T16E644-50-SAM-T | 128MB | 50 ns | KM44V16104AS-5/BS-5/CS-5 | TSOP | 32Mx32 | 16Mx4 | Samsung |
| 128T16E644-50-GS-T | 128MB | 50 ns | GM71V64403CT5 | TSOP | 32Mx32 | 16Mx4 | Goldstar |



Pin Assignment, (72 pin SIMM)

| Pin | Symbol | Pin | Symbol |
|-----|--------|-----|--------|
| 1 | Vss | 37 | NC |
| 2 | DQ0 | 38 | NC |
| 3 | DQ18 | 39 | Vss |
| 4 | DQ1 | 40 | CAS0* |
| 5 | DQ19 | 41 | CAS2* |
| 6 | DQ2 | 42 | CAS3* |
| 7 | DQ20 | 43 | CAS1* |
| 8 | DQ3 | 44 | RAS0* |
| 9 | DQ21 | 45 | RAS1* |
| 10 | Vcc | 46 | NC |
| 11 | NC | 47 | W* |
| 12 | A0 | 48 | NC |
| 13 | A1 | 49 | DQ9 |
| 14 | A2 | 50 | DQ27 |
| 15 | A3 | 51 | DQ10 |
| 16 | A4 | 52 | DQ28 |
| 17 | A5 | 53 | DQ11 |
| 18 | A6 | 54 | DQ29 |
| 19 | A10 | 55 | DQ12 |
| 20 | DQ4 | 56 | DQ30 |
| 21 | DQ22 | 57 | DQ13 |
| 22 | DQ5 | 58 | DQ31 |
| 23 | DQ23 | 59 | Vcc |
| 24 | DQ6 | 60 | DQ32 |
| 25 | DQ24 | 61 | DQ14 |
| 26 | DQ7 | 62 | DQ33 |
| 27 | DQ25 | 63 | DQ15 |
| 28 | A7 | 63 | DQ34 |
| 29 | A11 | 65 | DQ!6 |
| 30 | Vcc | 66 | NC |
| 31 | A8 | 67 | PD1 |
| 32 | A9 | 68 | PD2 |
| 33 | RAS3* | 69 | PD3 |
| 34 | RAS2* | 70 | PD4 |
| 35 | NC | 71 | NC |
| 36 | NC | 72 | Vss |

Pin Names

| Pin Name | Function |
|-----------------------------------|-------------------------------------|
| A0 – A11 | Address Inputs |
| DQ0-7, DQ9-16 DQ18-25, DQ27-34 | Data In/Out |
| W* | Read/Write Enable* (active low) |
| RAS0*-RAS3* | Row Address strobes (active low) |
| CAS0*-CAS3* | Column Address Strobes (active low) |
| PD1-PD4 | Presence Detect |
| Vcc | Power (+3.3/5V) |
| Vss | Ground |
| NC | No Connect |

Presence Detect Pins Options

| Pin | 50 nS | 60 nS |
|-----|-------|-------|
| PD1 | NC | NC |
| PD2 | Vss | Vss |
| PD3 | Vss | NC |
| PD4 | Vss | NC |

ABSOLUTE MAXIMUM RATINGS *

| Item | Symbol | Rating | Unit |
|--------------------------------------|------------------------------------|-------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -1 to +7.0 | V |
| Voltage on VCCsupply relative to Vss | V _{CC} | -1 to +7.0 | V |
| Storage Temperature | T _{stg} | -55 to +125 | °C |
| Power Dissipation | P _d | 16 | W |
| Short Circuit Output Current | I _{OS} | 50 | mA |

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta= 0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|--------------------|-----------------|--------|-----|--------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.4 | - | V _{CC} *1 | V |
| Input Low Voltage | V _{IL} | -1.0*2 | - | 0.8 | V |

*1 : V_{CC}+2.0V at pulse width £20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width £20ns, which is measured at V_{SS}.

The following DC and AC parameters are typical. Differences may exist from one memory device vendor to another as well as small differences from one die revision to another.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Symbol | Speed | Min | Max | Units |
|-------------------|------------|-----|------|-------|
| I _{CC1} | 50 nS | - | 1216 | mA |
| | 60 nS | - | 1136 | mA |
| I _{CC2} | Don't care | - | 32 | mA |
| I _{CC3} | 50 nS | - | 1216 | mA |
| | 60 nS | - | 1136 | mA |
| I _{CC4} | 50 nS | - | 976 | mA |
| | 60 nS | - | 656 | mA |
| I _{CC5} | Don't care | | 16 | mA |
| I _{CC6} | 50 nS | - | 1216 | mA |
| | 60 nS | - | 1136 | mA |
| I _{I(L)} | Don't care | -10 | 10 | uA |
| I _{O(L)} | | -5 | 5 | uA |
| V _{OH} | Don't care | 2.4 | - | V |
| V _{OL} | | - | 0.4 | V |

I_{CC1}: Operating Current* (RAS*, CAS*, Address cycling @t_{RC}=min)

I_{CC2}: Standby Current (RAS*=CAS*=W*=V_{in})

I_{CC3}: RAS* Only Refresh Current* (CAS*=V_{IH}, RAS* cycling @t_{RC}=min)

I_{CC4}: Hyper Page Mode Current* (RAS*=V_{IL}, CAS* cycling: t_{HPC}=min)

I_{CC5}: Standby Current (RAS*=CAS*=W*=V_{CC}-0.2V)

I_{CC6}: CAS*-before-RAS* Refresh Current* (RAS* and CAS* cycling @ t_{RC}=min)

I_{I(L)}: Input leakage current (Any input 0 ≤ V_{IN} ≤ V_{CC}+0.5V, all other input pins not under test = 0V)

I_{O(L)}: Output leakage Current (DataOut is disabled. 0V ≤ V_{out} ≤ V_{CC})

V_{OH}: Output high Voltage Level (I_{OH} = -5mA)

V_{OL}: Output Low Voltage Level (I_{OL} = 4.2 mA)

CAPACITANCE (TA = 25°C, VCC=5V, f=1MHZ)

| Item | Symbol | Min | Max | Unit |
|--|--------|-----|-----|------|
| Input capacitance[A0-A11] | CIN1 | - | 90 | pF |
| Input capacitance[W] | CIN2 | - | 122 | pF |
| Input capacitance[RAS0, RAS2] | CIN3 | - | 38 | pF |
| Input capacitance[CAS0 – CAS3] | CIN4 | - | 38 | pF |
| Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34] | CDQ | - | 17 | pF |

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V+/-10%)

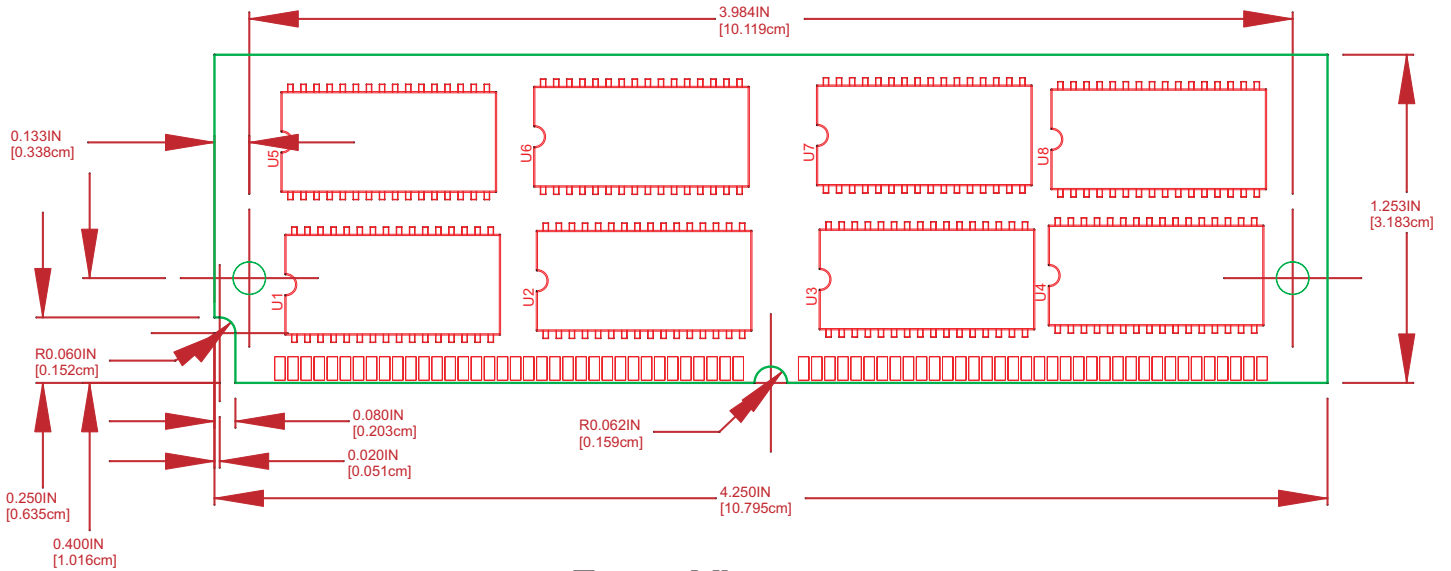
| Parameter | Symbol | 50 nS | | 60 nS | | Unit | Note |
|---|--------|-------|-----|-------|-----|------|--------|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 90 | | 110 | | ns | |
| Access time from RAS | tRAC | | 50 | | 60 | ns | 3,4,10 |
| Access time from CAS | tCAC | | 13 | | 15 | ns | 3,4,5 |
| Access time from column address | tAA | | 25 | | 30 | ns | 3,10 |
| CAS to output in Low-Z | tCLZ | 3 | | 3 | | ns | 3 |
| Output buffer turn-off delay from CAS | tCEZ | 3 | 13 | 3 | 13 | ns | 6,12 |
| Transition time(rise and fall) | tT | 1 | 50 | 1 | 50 | ns | 2 |
| RAS precharge time | tRP | 30 | | 40 | | ns | |
| RAS pulse width | tRAS | 50 | 10K | 60 | 10K | ns | |
| RAS hold time | tRSH | 13 | | 15 | | ns | |
| CAS hold time | tCSH | 38 | | 45 | | ns | |
| CAS pulse width | tCAS | 8 | 10K | 10 | 10K | ns | 4 |
| RAS to CAS delay time | tRCD | 20 | 37 | 20 | 45 | ns | 9 |
| RAS to column address delay time | tRAD | 15 | 25 | 15 | 30 | ns | |
| CAS to RAS precharge time | tCRP | 5 | | 5 | | ns | |
| Row address set-up time | tASR | 0 | | 0 | | ns | |
| Row address hold time | tRAH | 10 | | 10 | | ns | |
| Column address set-up time | tASC | 0 | | 0 | | ns | |
| Column address hold time | tCAH | 8 | | 10 | | ns | |
| Column address to RAS lead time | tRAL | 25 | | 30 | | ns | |
| Read command set-up time | tRCS | 0 | | 0 | | ns | |
| Read command hold referenced to CAS | tRCH | 0 | | 0 | | ns | 8 |
| Read command hold referenced to RAS | tRRH | 0 | | 0 | | ns | 8 |
| Write command set-up time | tWCS | 0 | | 0 | | ns | 7 |
| Write command hold time | tWCH | 10 | | 10 | | ns | |
| Write command pulse width | tWP | 10 | | 10 | | ns | |
| Write command to RAS lead time | tRWL | 13 | | 15 | | ns | |
| Write command to CAS lead time | tCWL | 8 | | 10 | | ns | |
| Data set-up time | tDS | 0 | | 0 | | ns | 9 |
| Data hold time | tDH | 8 | | 10 | | ns | 9 |
| Refresh period | tREF | | 64 | | 64 | ms | |
| CAS setup time (CAS-before-RAS refresh) | tCSR | 5 | | 5 | | ns | |
| CAS hold time (CAS-before-RAS refresh) | tCHR | 10 | | 10 | | ns | |
| RAS to CAS precharge time | tRPC | 5 | | 5 | | ns | |
| Access time from CAS precharge | tCPA | | 28 | | 35 | ns | 3 |

AC CHARACTERISTICS (continued)

| Parameter | Symbol | 50 nS | | 60 nS | | Unit | Note |
|--|--------|-------|------|-------|------|------|------|
| | | Min | Max | Min | Max | | |
| Hyper page mode cycle time | tHPC | 25 | | 30 | | ns | 11 |
| CAS precharge time (Hyper page cycle) | tCP | 8 | | 10 | | ns | |
| Access time from CAS (Hyper page cycle) | tCACP | | 15 | | 15 | | |
| Access time from col. Address (Hyper page cycle) | tAAP | | 25 | | 30 | | |
| RAS pulse width (Hyper page cycle) | tRASP | 50 | 200K | 60 | 200K | ns | |
| RAS hold time from CAS precharge | tRHCP | 30 | | 35 | | ns | |
| W to RAS precharge time(C-B-R refresh) | tWRP | 10 | | 10 | | ns | |
| W to RAS hold time(C-B-R refresh) | tWRH | 10 | | 10 | | ns | |
| Output data hold time | tDOH | 5 | | 5 | | ns | |
| Output buffer turn off delay from RAS | tREZ | 3 | 13 | 3 | 15 | ns | 6,12 |
| Output buffer turn off delay from W | tWEZ | 3 | 13 | 3 | 15 | ns | 6 |
| W to data delay | tWED | 15 | | 15 | | ns | |
| W pulse width | tWPE | 5 | | 5 | | ns | |

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il} . $V_{ih}(\min)$ and $V_{il}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{ih}(\min)$ and $V_{il}(\max)$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL} .
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS leading edge in early write cycles.
10. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit access time is controlled by t_{AA} .
11. $t_{ASC} \geq 6ns$, Assume $t_T = 2.0ns$.
12. If RAS goes high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes high before RAS high going, the open circuit condition of the output is achieved by RAS going.



Front View

NOTE: All dimensions in inches (cm).

All information in this data sheet is considered final, however, Memory Ten reserves the right to make changes as necessary.