

MemoryTen

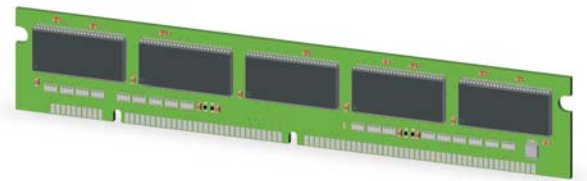
512U16S328-75DS-Q 64 Meg X 64 STACKED CHIP SDRAM 168 Pin DIMM PC-133

Features

- PC133-compliant, 168-pin, Dual in-line memory module (DIMM)
- Utilizes 143 MHz SDRAM components
- Unbuffered
- 512MB (64 Meg x 64)
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/ precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode: Standard and Low Power
- 64ms, 8,192-cycle, (7.8125µs) refresh interval
- LVTTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)
- Gold edge contacts

168-Pin DIMM (MO-161)

.943" tall



Parameter	512MB
Refresh Count	8K
Device Banks	4 (BA0, BA1)
Device Configuration	512Mb (64 Meg x 8)
Row Addressing	8K (A0–A12)
Column Addressing	2K (A0–A9, A11)
Module Ranks	2 (S0#, S2#; S1#, S3#)

PRODUCTION DATA information is current as of publication date.
 Products conform to specifications per the terms of MemoryTen
 standard warranty. Production processing does not necessarily include
 testing of all parameters.

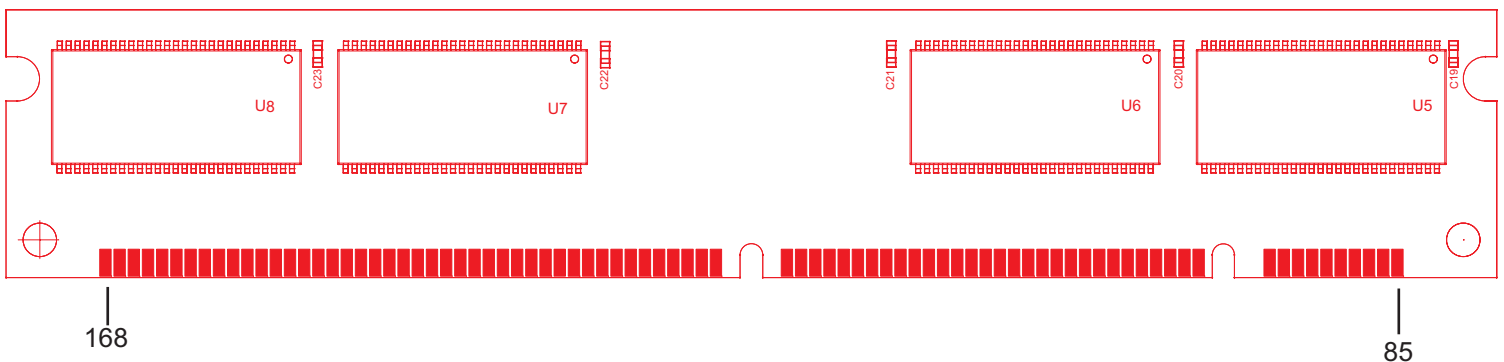
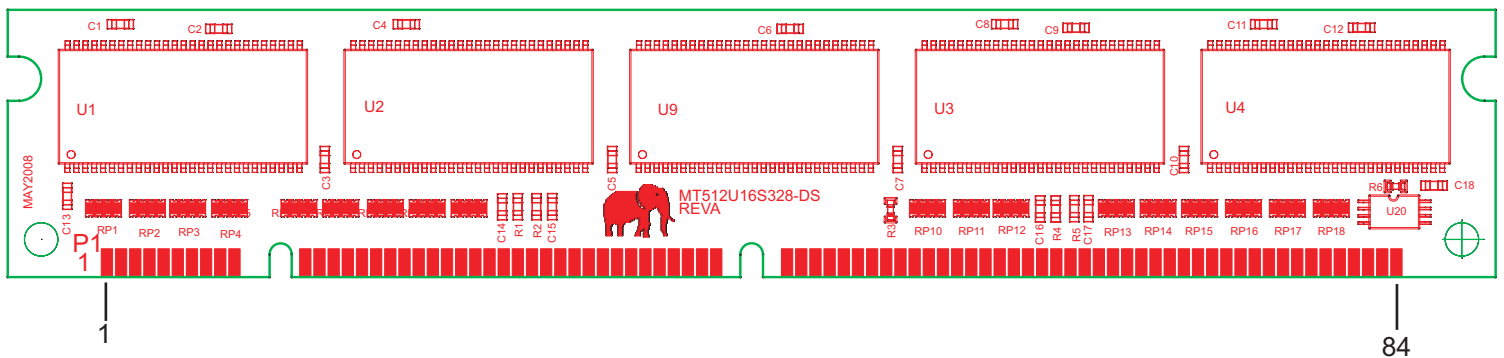
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ALL SPECIFICATIONS FOR PRODUCTS DISCUSSED HEREIN ARE SUBJECT TO CHANGE BY MemoryTen WITHOUT NOTICE.

ORDERING INFORMATION

PART NUMBER	MODULE DENSITY	CONFIGURATION	SYSTEM BUS SPEED
512U16S328-75DS-Q	512MB	64 Meg x 64	133 MHz

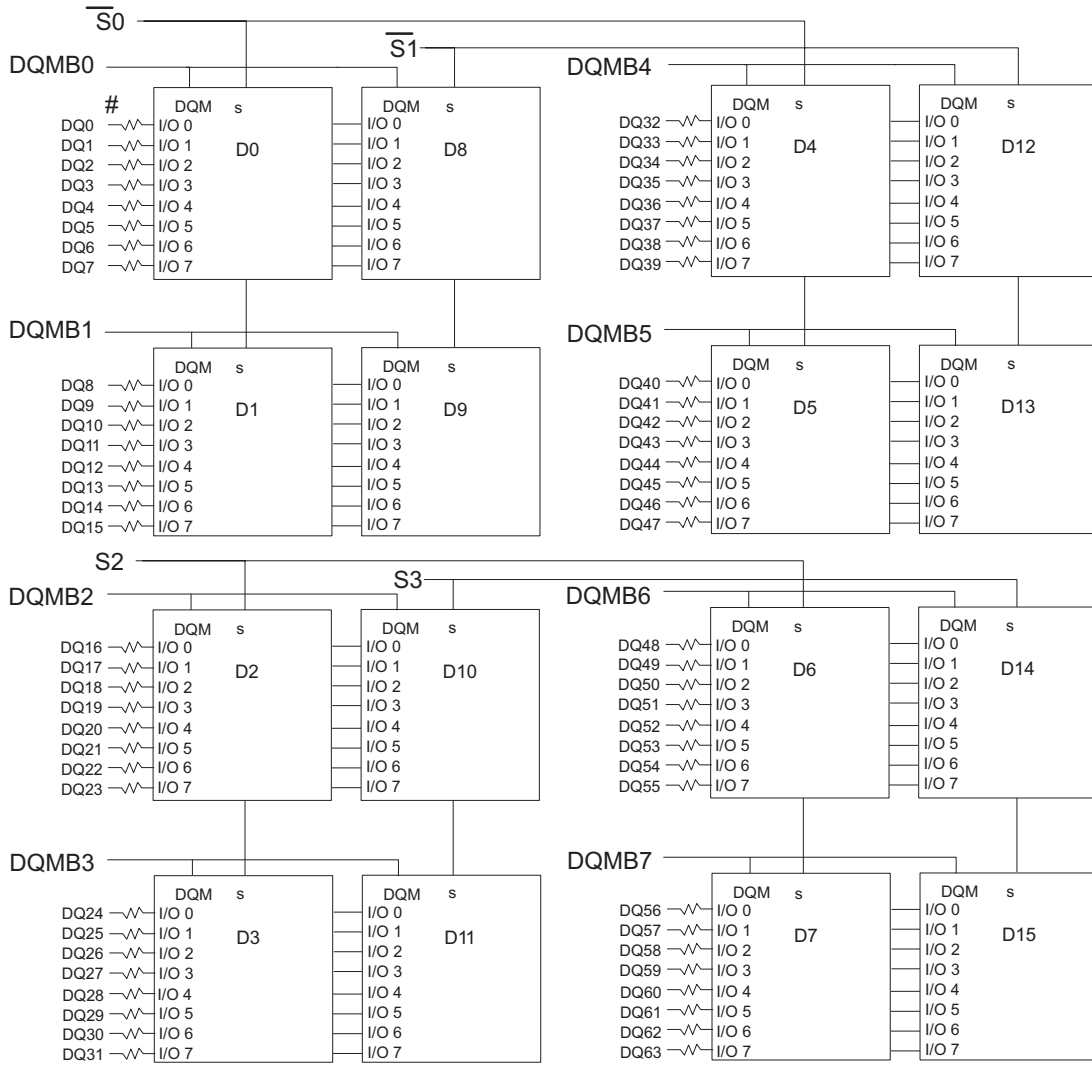
168-Pin DIMM Front								168-Pin DIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	22	NC	43	VSS	64	VSS	85	VSS	106	NC	127	VSS	148	VSS
2	DQ0	23	VSS	44	NC	65	DQ21	86	DQ32	107	VSS	128	CKE0	149	DQ53
3	DQ1	24	NC	45	S2#	66	DQ22	87	DQ33	108	NC	129	S3#	150	DQ54
4	DQ2	25	NC	46	DQMB2	67	DQ23	88	DQ34	109	NC	130	DQMB6	151	DQ55
5	DQ3	26	VDD	47	DQMB3	68	VSS	89	DQ35	110	VDD	131	DQMB7	152	VSS
6	VDD	27	WE#	48	NC	69	DQ24	90	VDD	111	CAS#	132	NC	153	DQ56
7	DQ4	28	DQMB0	49	VDD	70	DQ25	91	DQ36	112	DQMB4	133	VDD	154	DQ57
8	DQ5	29	DQMB1	50	NC	71	DQ26	92	DQ37	113	DQMB5	134	NC	155	DQ58
9	DQ6	30	S0#	51	NC	72	DQ27	93	DQ38	114	S1#	135	NC	156	DQ59
10	DQ7	31	NC	52	NC	73	VDD	94	DQ39	115	RAS#	136	NC	157	VDD
11	DQ8	32	VSS	53	NC	74	DQ28	95	DQ40	116	VSS	137	NC	158	DQ60
12	VSS	33	A0	54	VSS	75	DQ29	96	VSS	117	A1	138	VSS	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	VSS	99	DQ43	120	A7	141	DQ50	162	VSS
16	DQ12	37	A8	58	DQ19	79	CK2	100	DQ44	121	A9	142	DQ51	163	CK3
17	DQ13	38	A10	59	VDD	80	NC	101	DQ45	122	BA0	143	VDD	164	NC
18	VDD	39	BA1	60	DQ20	81	NC	102	VDD	123	A11	144	DQ52	165	SA0
19	DQ14	40	VDD	61	NC	82	SDA	103	DQ46	124	VDD	145	NC	166	SA1
20	DQ15	41	VDD	62	NC	83	SCL	104	DQ47	125	CK1	146	NC	167	SA2
21	NC	42	CK0	63	CKE1	84	VDD	105	NC	126	A12	147	NC	168	VDD



Pin Descriptions

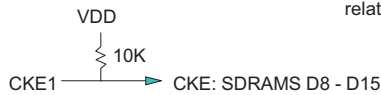
Pin Numbers	Symbol	Type	Description
27, 111, 115	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
42, 79, 125, 163	CK0–CK3	Input	Clock: CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
63, 128	CKE0, CKE1	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all device banks idle) or CLOCK SUSPEND OPERATION (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power.
30, 45, 114, 129	S0#–S3#	Input	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
28, 29, 46, 47, 112, 113, 130, 131	DQMB0–DQMB7	Input	Input/Output mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
39, 122	BA0, BA1	Input	Bank address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
33–38, 117–121, 123, 126	A0–A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command.
83	SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
165–167	SA0–SA2	Input	Presence-Detect address Inputs: These pins are used to configure the presence-detect device.
2–5, 7–11, 13–17, 19–20, 55–58, 60, 65–67, 69–72, 74–77, 86–89, 91–95, 97–101, 103–104, 139–142, 144, 149–151, 153–156, 158–161	DQ0–DQ63	Input/Output	Data I/O: Data bus.
82	SDA	Input/Output	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	VDD	Supply	Power supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	VSS	Supply	Ground.

BLOCK DIAGRAM



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMs
*CK1	4 SDRAMs
*CK2	4 SDRAMs
*CK3	4 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

BA0 - BAN → BA0-BAN: SDRAMs D0 - D15

A0 - AN → A0-AN: SDRAMs D0 - D15

VDD → D0 - D15

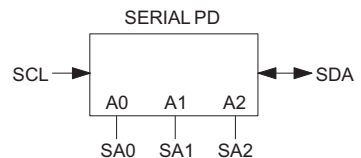
VSS → D0 - D15

RAS → RAS: SDRAMs D0 - D15

CAS → CAS: SDRAMs D0 - D15

CKE0 → CKE: SDRAMs D0 - D7

WE → WE: SDRAMs D0 - D15



NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Note: This module is built with stacked chips, thus, D0 and D8, D1 and D9, D2 and D10, D3 and D11, D4 and D12, D5 and D13, D6 and D14, D7 and D15 are paired in one stacked package.

X64 SDRAM DIMM, 2 Banks with X8 SDRAMs

Module Characteristics

DC Characteristics

$T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{DD}, V_{DDQ} = 3.3$ V \pm 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	$V_{CC}+0.3$	V
Input low voltage	V_{IL}	- 0.5	0.8	V
Output high voltage ($I_{OUT} = - 2.0$ mA)	V_{OH}	2.4	-	V
Output low voltage ($I_{OUT} = 2.0$ mA)	V_{OL}	-	0.4	V
Input leakage current, any input (0 V $< V_{IN} < 3.6$ V, all other inputs = 0 V)	$I_{I(L)}$	- 40	40	uA
Output leakage current (DQ is disabled, 0 V $< V_{OUT} < V_{CC}$)	$I_{O(L)}$	- 40	40	uA

Capacitance

$T_A = 0$ to 70 °C; $V_{DD} = 3.3$ V \pm 0.3 V, $f = 1$ MHz

Parameter	Symbol	Limit Values (max.)	Unit
Input capacitance (A0 to A10, BA, RAS, CAS, WE)	C_{I1}	80	pF
Input capacitance (CS0 -CS3)	C_{I2}	30	pF
Input capacitance (CLK0 - CLK3)	C_{ICL}	22	pF
Input capacitance (CKE0, CKE1)	C_{I3}	50	pF
Input capacitance (DQMB0 - DQMB7)	C_{I4}	20	pF
Input / Output capacitance (DQ0-DQ63)	C_{IO}	20	pF
Input Capacitance (SCL,SA0-2)	C_{Sc}	8	pF
Input/Output Capacitance	C_{Sd}	10	pF

I_{DD} SPECIFICATIONS

Standby and Refresh Currents (T_a = 0 to 70°C, V_{CC} = 3.3V ± 0.3V)

Parameter	Symbol	Test Condition	max.	Note	
Operating Current	I _{cc1}	Burst length = 4, CL=3 trc>=trc(min.), tck>=tck(min.), I _o =0 mA 2 bank interleave operation	800	mA	1,2
Precharged Standby	I _{cc2P}	CKE<=VIL(max), tck>=tck(min.)	24	mA	
Current in Power Down Mode	I _{cc2PS}	CKE<=VIL(max), tck=infinite	16	mA	
Precharged Standby Current in Non-power Down Mode	I _{cc2N}	CKE>=VIH(min), tck>=tck (min.), input changed once in 3 cycles	160	mA	CS= High
	I _{cc2NS}	CKE>=VIH(min), tck=infinite, no input change	80	mA	
Active Standby	I _{cc3P}	CKE<=VIL(max), tck>=tck(min.)	24	mA	
Current in Power Down Mode	I _{cc3PS}	CKE<=VIL(max), tck=infinite	16	mA	
Active Standby Current in Non-power Down Mode	I _{cc3N}	CKE>=VIH(min), tck>=tck (min.) input changed one time	200	mA	CS= High
	I _{cc3NS}	CKE>=VIH(min), tck=infinite, no input change	120	mA	
Burst Operating Current	I _{cc4}	Burst length = full page,	760	mA	1,2
		trc = infinite, CL = 3,			
		tck>=tck (min.), I _o = 0 mA 2 banks activated			
Auto (CBR) Refresh Current	I _{cc5}	trc>=trc(min)	720	mA	1,2
Self Refresh Current	I _{cc6}	CKE=<0,2V	16	mA	1,2

AC Characteristics

TA = 0 to 70 °C; VSS = 0 V; VCC = 3.3 V ± 0.3 V, fT = 1 ns

Parameter	Symbol	Limit Values		Unit
		-75 PC133 2-2-2		
		Min.	Max.	
Clock and Clock Enable				
Clock Cycle Time CAS Latency = 3 CAS Latency = 2	t_{CK}			
		7.7		ns
		7		ns
System Frequency CAS Latency = 3 CAS Latency = 2	f_{CK}			
		–	133	MHz
		–	133	MHz
Clock Access Time CAS Latency = 3 CAS Latency = 2	t_{AC}			
		–	5.4	ns
		–	5.4	ns
Clock High Pulse Width	t_{CH}	2.5	–	ns
Clock Low Pulse Width	t_{CL}	2.5	–	ns
Input Setup time	t_{CS}	1.5	–	ns
Input Hold time	t_{CH}	.8	–	ns
CKE Setup Time (Power Down Mode)	t_{CKSP}	1.5	–	ns
CKE Setup Time (Self Refresh Mode)	t_{CKSR}	6	–	ns
Transition Time (rise and fall)	t_T	1	–	ns
Common Parameters				
RAS to CAS delay	t_{RCD}	15	–	ns
Cycle Time	t_{RC}	60	120k	ns
Active Command Period	t_{RAS}	37	–	ns
Precharge Time	t_{RP}	15	–	ns
Bank to Bank Delay Time	t_{RRD}	16	–	ns
CAS to CAS delay time (same bank)	t_{CCD}	1	–	CLK

AC Characteristics (continued)

Parameter	Symbol	Limit Values		Unit
		-75 PC133 2-2-2		
		Min.	Max.	
Refresh Cycle				
Self Refresh Exit Time	t_{SREX}	10	–	ns
Refresh Period (4096 cycles)	t_{REF}	64	–	ms
Refresh Period (8192 cycles)	t_{REF}	64	–	ms
Read Cycle				
Data Out Hold Time	t_{OH}	2.7	–	ns
Data Out to Low Impedance Time	t_{LZ}	1	–	ns
Data Out to High Impedance Time	t_{HZ}	3	9	ns
DQM Data Out Disable Latency	t_{DQZ}	2	–	CLK
Write Cycle				
Data input to Precharge(write Recovery)	t_{DPL}	2	–	CLK
Data In to Active/refresh	t_{DAL}	2	–	CLK
DQM Write Mask Latency	t_{DQW}	0	–	CLK

Notes:

1. The specified values are valid when addresses are changed no more than once during $t_{ck}(\text{min.})$ and when No Operation commands are registered on every rising clock edge during $t_{RC}(\text{min.})$. Values are shown per module bank.
2. The specified values are valid when data inputs (DQs) are stable during $t_{RC}(\text{min.})$.
3. All AC characteristics are shown for device level.
An initial pause of 100ns is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have $V_{il} = 0.4\text{ V}$ and $V_{ih} = 2.4\text{ V}$ with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il} . All AC measurements assume $t_T = 1\text{ ns}$ with the AC output load circuit show. Specified t_{ac} and t_{oh} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1 V / ns edge rate between 0.8 V and 2.0 V .

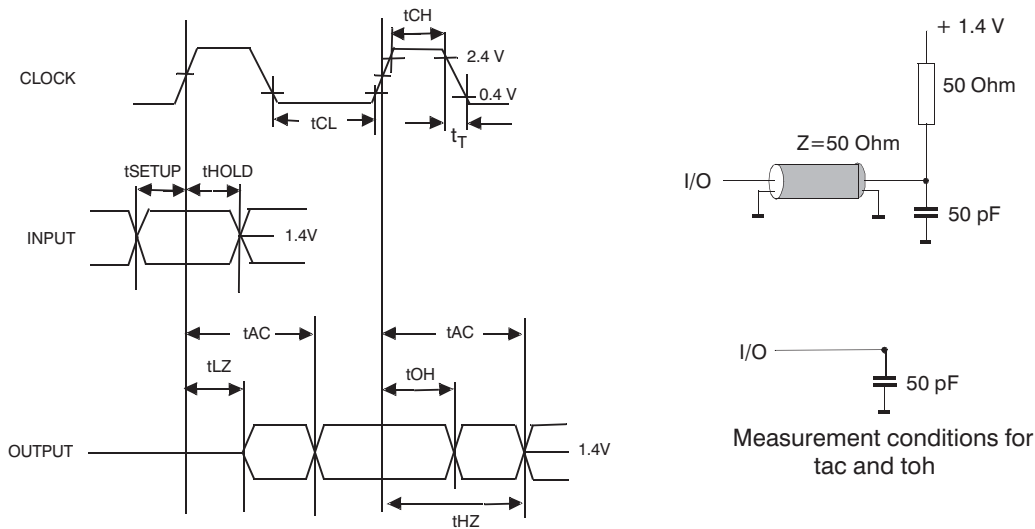


fig.1

5. If clock rising time is longer than 1 ns , a time $(t_T/2 - 0.5)\text{ ns}$ has to be added to this parameter.
6. Rated at 1.5 V
7. If t_T is longer than 1 ns , a time $(t_T - 1)\text{ ns}$ has to be added to this parameter.
8. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
11. t_{DAL} is equivalent to $t_{DPL} + t_{RP}$.

Serial Presents Detect (SPD)

D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Units
I _{CCR}	Read Current	Read, f _{SCL} = 400kHz		1	mA
I _{CCW}	Write Current	Write, f _{SCL} = 400kHz		2	mA
I _{SB}	Standby Current	All I/O Pins at GND or V _{CC}	T _A = -40°C to +85°C	1	μA
			T _A = -40°C to +125°C	2	
I _L	I/O Pin Leakage	Pin at GND or V _{CC}	T _A = -40°C to +85°C	1	μA
			T _A = -40°C to +125°C	2	
V _{IL}	Input Low Voltage		-0.5	V _{CC} × 0.3	V
V _{IH}	Input High Voltage		V _{CC} × 0.7	V _{CC} + 0.5	V
V _{OL1}	Output Low Voltage	V _{CC} < 2.5 V, I _{OL} = 3.0mA		0.4	V
V _{OL2}	Output Low Voltage	V _{CC} < 2.5 V, I _{OL} = 1.0mA		0.2	V

PIN IMPEDANCE CHARACTERISTICS

--	Parameter	Conditions	Max	Units
C _{IN}	SDA I/O Pin Capacitance	V _{IN} = 0 V	8	pF
C _{IN}	Input Capacitance (other pins)	V _{IN} = 0 V	6	pF
I _{WP}	WP Input Current	V _{IN} < V _{IH} , V _{CC} = 5.5 V	200	μA
		V _{IN} < V _{IH} , V _{CC} = 3.3 V	150	
		V _{IN} < V _{IH} , V _{CC} = 1.8 V	100	
		V _{IN} > V _{IH}	1	

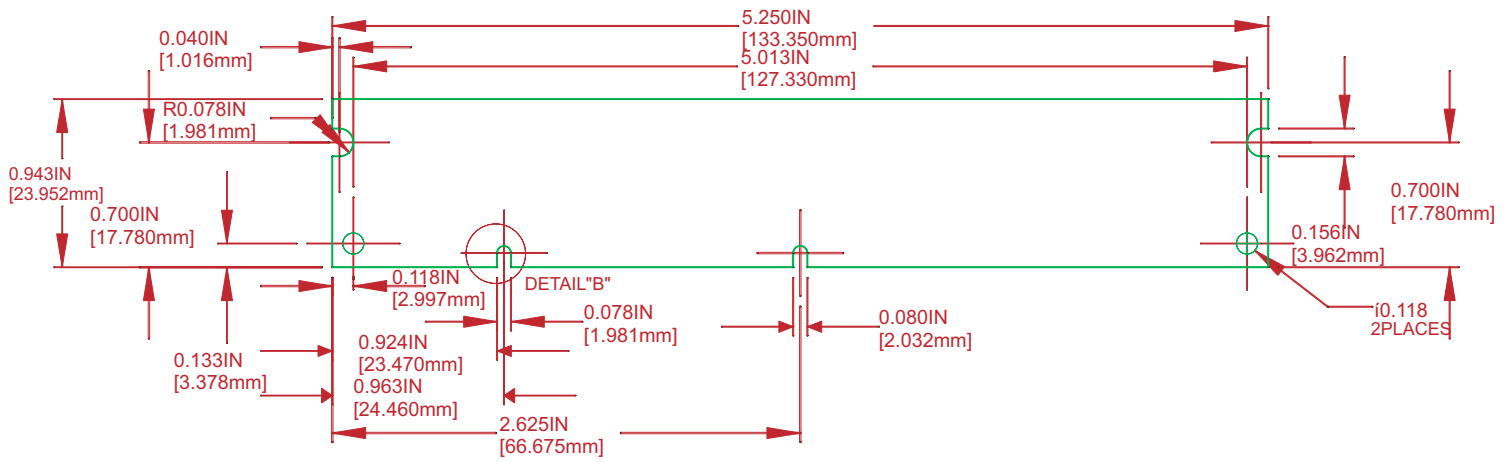
A.C. CHARACTERISTICS^①

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C.

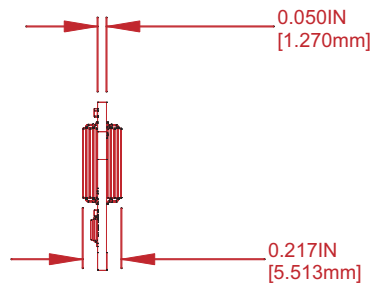
Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
SCL	Clock Frequency		100		400	kHz
t _{HD:STA}	START Condition Hold Time	4		0.6		μs
t _{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t _{HIGH}	High Period of SCL Clock	4		0.6		μs
t _{SU:STA}	START Condition Setup Time	4.7		0.6		μs
t _{HD:DAT}	Data In Hold Time	0		0		μs
t _{SU:DAT}	Data In Setup Time	250		100		ns
t _R	SDA and SCL Rise Time		1000		300	ns
t _F	SDA and SCL Fall Time		300		300	ns
t _{SU:STO}	STOP Condition Setup Time	4		0.6		μs
t _{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
t _{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t _{DH}	Data Out Hold Time	100		100		ns
T _i	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
t _{SU:WP}	WP Setup Time	0		0		μs
t _{HD:WP}	WP Hold Time	2.5		2.5		μs
t _{WR}	Write Cycle Time		5		5	ms
t _{PU}	Power-up to Ready Mode		1		1	ms

A.C. TEST CONDITIONS

Input Levels	0.2 x V _{CC} to 0.8 x V _{CC}
Input Rise and Fall Times	≤50 ns
Input Reference Levels	0.3 x V _{CC} , 0.7 x V _{CC}
Output Reference Levels	0.5 x V _{CC}
Output Load	Current Source: I _{OL} = 3 mA (V _{CC} ≥ 2.5 V); I _{OL} = 1 mA (V _{CC} < 2.5 V); C _L = 100 pF



FRONT VIEW



END VIEW

NOTE: All dimensions in inches (cm).

All information in this data sheet is considered final, however, Memory Ten reserves the right to make changes as necessary.