

# MemoryTen

1GM8T1288-533MT 128 Meg X 64 DDR2 172 Pin microDIMM PC-4200

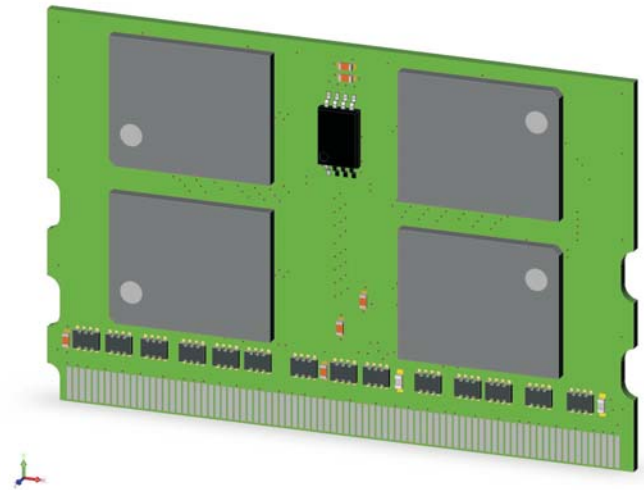
512M8T648-533MT 64 Meg X 64 DDR2 172 Pin microDIMM PC-4200

## Features

- PC4200-compliant, 172-pin, microDIMM
- Utilizes 533 (266MHZ CLK) MHZ DDR2 SDRAM components
- Unbuffered
- 512MB (64 Meg x 64), 1GB (128 Meg x 64)
- Single +1.8V power supply
- VDDSPD = 2.5V TO 3.6v
- Differential Clock
- 4n-bit prefetch
- 4 Internal SDRAM banks for concurrent access operation
- DLL to align DQ and DQS transitions with CK
- Bidirectional differential data strobe (DQS, DQS#) source-synchronous data capture
- Programmable burst lengths: 4, or 8
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 8,192 cycle (7.8125µs) refresh interval
- 1.8v SSTTL\_18-compatible inputs and outputs
- Serial Presence-Detect (SPD)
- Gold edge contacts
- Selectable CAS latency
- On-die termination

## 172-Pin SODIMM (MO-214)

1.118" tall



Representative illustration, actual configuration may vary due to different packages from different vendors.

## ADDRESSING

Parameter	512MB	1GB
Refresh count	8K	8K
Row address	8K (A0–A12)	16K (A0–A13)
Device bank address	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K(A0-A9)	2K(A0-A9, A11)
Module rank address	1 (S0#)	1 (S0#)

PRODUCTION DATA information is current as of publication date.  
 Products conform to specifications per the terms of MemoryTen  
 standard warranty. Production processing does not necessarily include  
 testing of all parameters.

ALL SPECIFICATIONS FOR PRODUCTS DISCUSSED HEREIN ARE SUBJECT TO CHANGE BY MemoryTen WITHOUT NOTICE.

## General Description

The 512M8T648-533MT and 1GN8T1288-533MT are a high-speed, CMOS, dynamic random access 512MB, and 1GB memory module organized in a x64 configuration. DDR2 SDRAM devices use internally configured, 8-bank 512Mb DDR2 SDRAM devices.

DDR2 SDRAM modules transmit data on both the rising and falling edge of the clock ( double data rate architecture) to achieve high-speed operation.

A differential bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS, DQS# is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS, DQS# is edge-aligned with data for

READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK.

Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS,DQS#, and output data is referenced to both edges of DQS,DQS# as well as to both edges of CK.

### Key Timing Parameters

Industry Nomenclature	Data Rate (MT/s)			tRCD (ns)	tRP (ns)	tRC (ns)
	CL = 3	CL =4	CL = 5			
PC4200	–	533	533	15	15	55

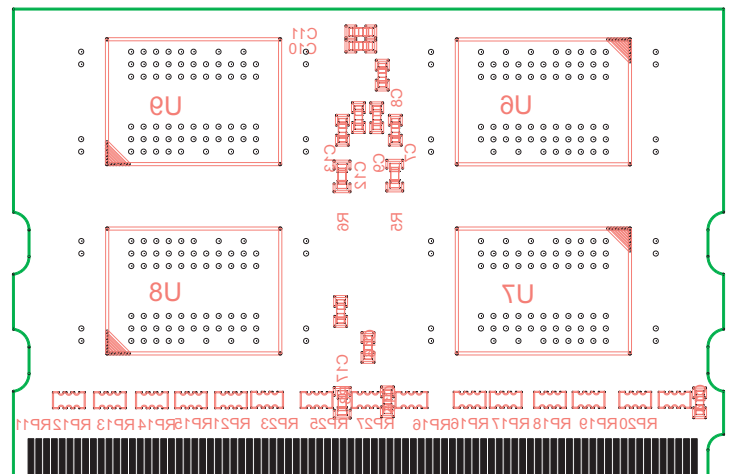
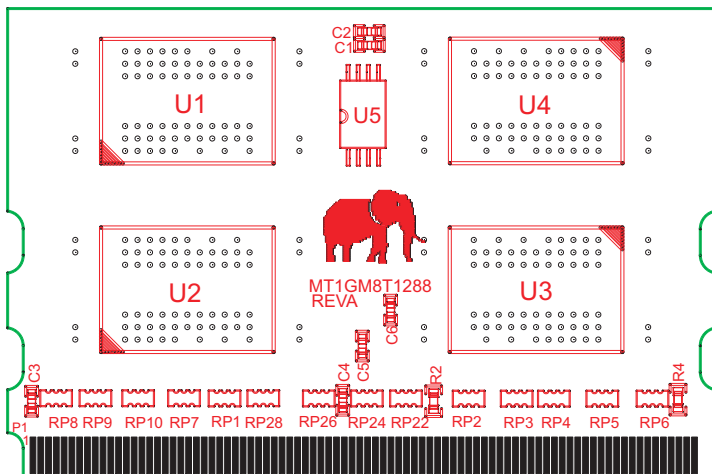
Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate
512M8T648-533MT	512MB	64 Meg x 64	4.2 GB/s	3.75ns/533 MT/s
1GM8T1288-533MT	1GB	128 Meg X 64	4.2 GB/s	3.75ns/533 MT/s

## Pin Assignment (172-Pin MICRODIMM)

172-Pin DDR2 MICRODIMM Front					
Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	59	DQ27	117	DQ34
3	DQ0	61	Vss	119	DQ36
5	DQ1	63	CK0	121	Vss
7	Vss	65	/CK0	123	DQ40
9	/DQS0	67	Vss	125	DQ41
11	DQS0	69	CKE0	127	Vss
13	Vss	71	Vdd	129	DM5
15	DQ2	73	A1	131	DQ42
17	DQ3	75	Vdd	133	DQ43
19	DQ8	77	A3	135	VSS
21	DQ9	79	A5	137	DQ48
23	Vss	81	Vdd	139	DQ49
25	DM1	83	A7	141	Vss
27	DQ10	85	A9	143	/DQS6
29	DQ11	87	A12	145	DQS5
31	Vss	89	VDD	147	VSS
33	DQ16	91	A10/AP	149	DQ50
35	DQ17	93	BA0	151	DQ51
37	Vss	95	/CAS	153	Vss
39	/DQS2	97	Vdd	155	DQ56
41	DQS2	99	/CS1	157	DQ57
43	Vss	101	/WE	159	VSS
45	DQ18	103	Vdd	161	DM7
47	DQ19	105	ODT1	163	DQ58
49	DQ24	107	Vss	165	DQ59
51	DQ25	109	DQ32	167	Vss
53	Vss	111	DQ33	169	SDA
55	DM3	113	Vss	171	VDDSPD
57	DQ26	115	DM4		

## Pin Assignment (172-Pin MICRODIMM)

172-Pin DFDR2 MICRODIMM Back					
Pin	Symbol	Pin	Symbol	Pin	Symbol
2	VREF	60	VSS	118	VSS
4	VSS	62	DQ30	120	DQ38
6	DQ4	64	DQ31	122	DQ39
8	DQ5	66	VSS	124	DQ44
10	DM0	68	CKE1	126	DQ45
12	VSS	70	VDD	128	VSS
14	DQ6	72	A0	130	/DQS5
16	DQ7	74	VDD	132	DQS5
18	VSS	76	A2	134	VSS
20	DQ12	78	A4	136	DQ46
22	DQ13	80	VDD	138	DQ47
24	VSS	82	A6	140	DQ52
26	/DQS1	84	A8	142	DQ53
28	DQS1	86	A11	144	VSS
30	VSS	88	VDD	146	DM6
32	DQ14	90	A13	148	DQ54
34	DQ15	92	BA2	150	DQ56
36	DQ20	94	BA1	152	VSS
38	DQ24	96	VDD	154	DQ60
40	VSS	98	/CS0	156	DQ61
42	DM2	100	/RAS	158	VSS
44	DQ22	102	VDD	160	/DQS7
46	DQ23	104	ODT0	162	DQS7
48	VSS	106	VSS	164	VSS
50	DQ28	108	DQ36	166	DQ62
52	DQ29	110	DQ37	168	DQ63
54	VSS	112	VSS	170	VSS
56	/DQS3	114	/DQS4	172	SCL
58	DQS3	116	DQS4		



Pin 1

Pin 171 Pin 172

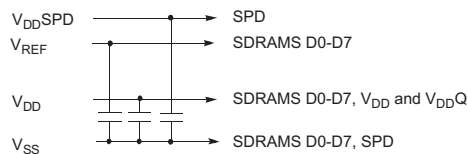
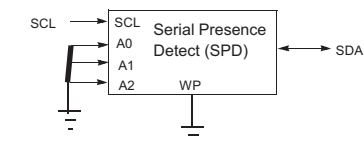
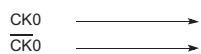
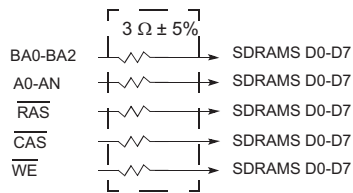
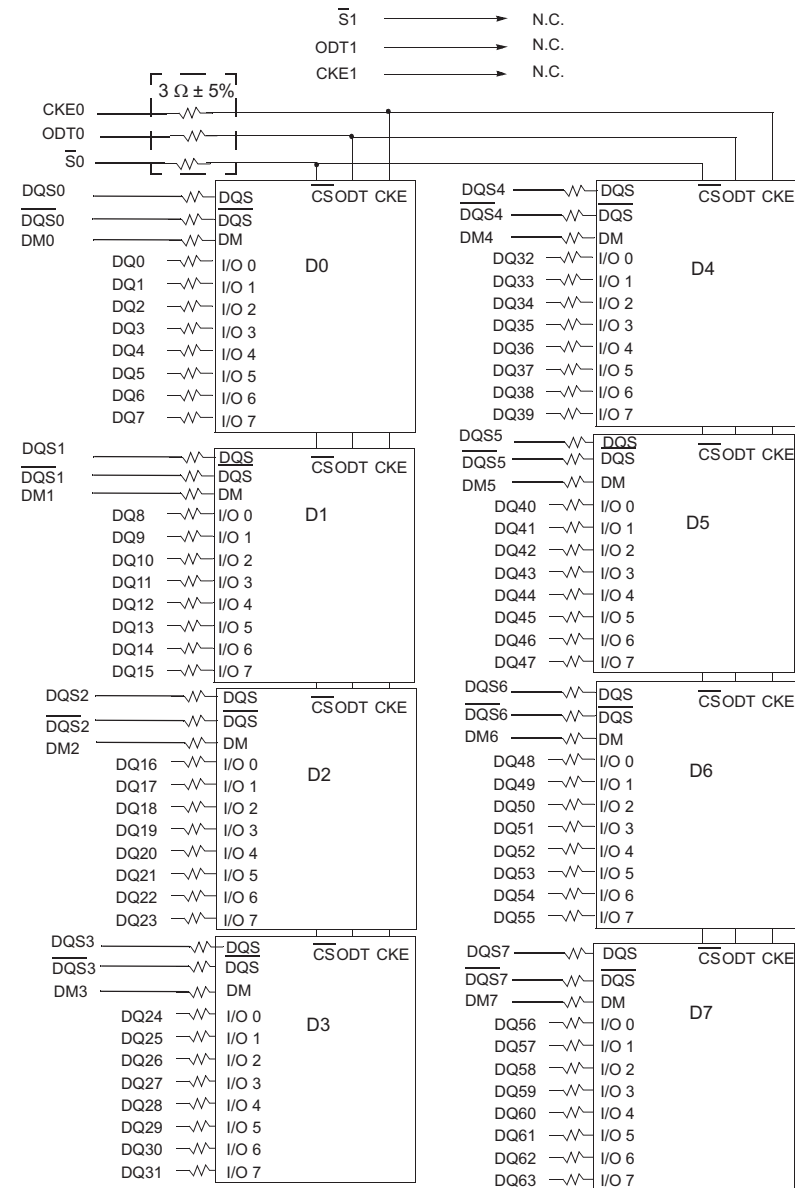
Pin 2

## Pin Descriptions

Symbol	Type	Description
A0–A12	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. A0–A11 (128MB), A0–A12 (256MB, 512MB), and A0–A13 (1GB).
BA0, BA1, BA2	Input	<b>Bank address:</b> BA0, BA1 and BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK0, CK0#,	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE0, CEK1	Input	<b>Clock enable:</b> CEK HIGH activates and CEK LOW deactivates the internal clock, input buffers, and output drivers.
DM0–DM7	Input	<b>Data write mask:</b> DM LOW enables WRITE operation. DM HIGH blocks WRITE operation. DM lines do not affect READ operation.
CS0#, CS1#	Input	<b>Chip selects:</b> CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# is considered part of the command code.
ODT0, ODT1	Input	<b>On Die Termination:</b> These pins are used to configure control the on die termination.
SCL	Input	<b>Serial clock for presence-detect:</b> SCL is used to synchronize the presence-detect data transfer to and from the module.
WE#, CAS#, RAS#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with S#) define the command being entered.
DQ0–DQ63	I/O	<b>Data I/Os:</b> Data bus.
DQS0–DQS7 /DQS0–DQS7	I/O	<b>Differential Data strobe:</b> Output with read data; input with write data. DQS is edge-aligned with read data, center-aligned with write data. Used to capture data.
SDA	I/O	<b>Serial presence-detect data:</b> SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
VDD	Supply	<b>Power supply:</b> +2.5V ±0.2V
VDDSPD	Supply	<b>Serial EEPROM positive power supply:</b> +2.3V to +3.6V.
VREF	Supply	SSTL_2 reference voltage (VDD/2).
VSS	Supply	Ground.
NC	–	<b>No connect:</b> These pins are not connected on the module.

# Block Diagram

512MB, 1GB: (x64, DR2) PC4200 172-Pin DDR2 MICRO DIMM



#Unless otherwise noted, resistor values are  $22\ \Omega - 5\%$   
 DQ wiring may differ from that described in this drawing; however, DQ/DM/DQS/DQS relationships are maintained as shown

# Module Characteristics

## Absolute Maximum Ratings

All voltages referenced to Vss.

Parameter	Absolute Maximum Value
VDDsupply voltage	-1V to +2.3V
VDDQ supply voltage	-.5V to +2.3V
VREFand inputs voltage	-.5V to +2.3V
I/O pins voltage	-0.5V to VDDQ +0.5V
Storage temperature (plastic)	-50°C to +100°C
Short circuit output current	50mA

## DC Characteristics

TA = 0 to 70 °C; VSS = 0 V; VDD, VDDQ = 2.5 V ± 0.2 V

Parameter/Condition	Symbol	Min	Max	Units	
Supply voltage	VDD	+1.7	+1.9	V	
I/O supply voltage	VDDQ	+1.7	+1.9	V	
I/O reference voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	
I/O termination voltage (at the system level)	VTT	VREF- 0.04	VREF+ 0.04	V	
Input high (logic 1) voltage	VIH(DC)	VREF+ 0.125	VDDQ+ 0.3	V	
Input low (logic 0) voltage	VIL(DC)	-0.3	VREF- 0.125	V	
Ambient operating temperatures	Commercial	TA	0	+70	°C

## Serial Presents Detect (SPD)

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit nonvolatile EEPROM configured as 2 blocks of 128 X 8 bits. The first 128 bytes are programmed by Memory Ten to identify the module type, SDRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device on the DIMM occur via a standard I2C bus using the DIMM's SCL (clock) and SDA (data) signals. SA0 - SA2 provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to VSS on the module, permanently disabling hardware write protect.

## D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Units
I <sub>CCR</sub>	Read Current	Read, f <sub>SCL</sub> =400kHz		1	mA
I <sub>CCW</sub>	Write Current	Write, f <sub>SCL</sub> =400kHz		2	mA
I <sub>SB</sub>	Standby Current	All I/O Pins at GND or V <sub>CC</sub>	T <sub>A</sub> = -40°C to +85°C	1	μA
			T <sub>A</sub> = -40°C to +125°C	2	
I <sub>L</sub>	I/O Pin Leakage	Pin at GND or V <sub>CC</sub>	T <sub>A</sub> = -40°C to +85°C	1	μA
			T <sub>A</sub> = -40°C to +125°C	2	
V <sub>IL</sub>	Input Low Voltage		-0.5	V <sub>CC</sub> x 0.3	V
V <sub>IH</sub>	Input High Voltage		V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 0.5	V
V <sub>OL1</sub>	Output Low Voltage	V <sub>CC</sub> < 2.5 V, I <sub>OL</sub> = 3.0mA		0.4	V
V <sub>OL2</sub>	Output Low Voltage	V <sub>CC</sub> < 2.5 V, I <sub>OL</sub> = 1.0mA		0.2	V

## PIN IMPEDANCE CHARACTERISTICS

--	Parameter	Conditions	Max	Units
C <sub>IN</sub>	SDA I/O Pin Capacitance	V <sub>IN</sub> = 0 V	8	pF
C <sub>IN</sub>	Input Capacitance (other pins)	V <sub>IN</sub> = 0 V	6	pF
I <sub>WP</sub>	WP Input Current	V <sub>IN</sub> < V <sub>IH</sub> , V <sub>CC</sub> = 5.5 V	200	μA
		V <sub>IN</sub> < V <sub>IH</sub> , V <sub>CC</sub> = 3.3 V	150	
		V <sub>IN</sub> < V <sub>IH</sub> , V <sub>CC</sub> = 1.8 V	100	
		V <sub>IN</sub> > V <sub>IH</sub>	1	

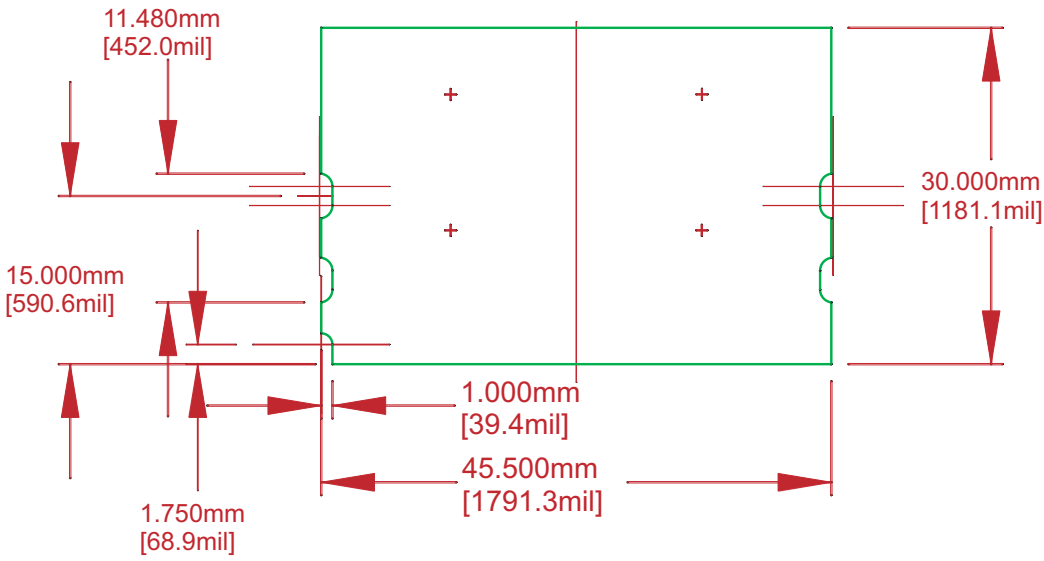
### A.C. CHARACTERISTICS<sup>①</sup>

V<sub>CC</sub> = 1.8 V to 5.5 V, T<sub>A</sub> = -40°C to +125°C.

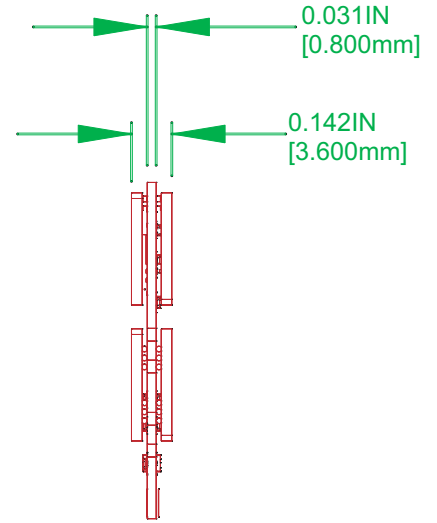
Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
SCL	Clock Frequency		100		400	kHz
t <sub>HD:STA</sub>	START Condition Hold Time	4		0.6		μs
t <sub>LOW</sub>	Low Period of SCL Clock	4.7		1.3		μs
t <sub>HIGH</sub>	High Period of SCL Clock	4		0.6		μs
t <sub>SU:STA</sub>	START Condition Setup Time	4.7		0.6		μs
t <sub>HD:DAT</sub>	Data In Hold Time	0		0		μs
t <sub>SU:DAT</sub>	Data In Setup Time	250		100		ns
t <sub>R</sub>	SDA and SCL Rise Time		1000		300	ns
t <sub>F</sub>	SDA and SCL Fall Time		300		300	ns
t <sub>SU:STO</sub>	STOP Condition Setup Time	4		0.6		μs
t <sub>BUF</sub>	Bus Free Time Between STOP and START	4.7		1.3		μs
t <sub>AA</sub>	SCL Low to Data Out Valid		3.5		0.9	μs
t <sub>DH</sub>	Data Out Hold Time	100		100		ns
T <sub>i</sub>	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
t <sub>SU:WP</sub>	WP Setup Time	0		0		μs
t <sub>HD:WP</sub>	WP Hold Time	2.5		2.5		μs
t <sub>WR</sub>	Write Cycle Time		5		5	ms
t <sub>PU</sub>	Power-up to Ready Mode		1		1	ms

### A.C. TEST CONDITIONS

Input Levels	0.2 x V <sub>CC</sub> to 0.8 x V <sub>CC</sub>
Input Rise and Fall Times	?50 ns
Input Reference Levels	0.3 x V <sub>CC</sub> , 0.7 x V <sub>CC</sub>
Output Reference Levels	0.5 x V <sub>CC</sub>
Output Load	Current Source: I <sub>OL</sub> = 3 mA (V <sub>CC</sub> ?2.5 V); I <sub>OL</sub> = 1 mA (V <sub>CC</sub> < 2.5 V); C <sub>L</sub> = 100 pF



**FRONT VIEW**



**END VIEW**

**NOTES:**

1. All dimensions in mm[inches].
2. The above diagram is for reference only. Refer to JEDEC MO document for additional dimensions.

All information in this data sheet is considered final, however, Memory Ten reserves the right to make changes as necessary.